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Delivering Excellence in Semiconductor Engineering

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FROM THE PRESIDENT'S DESK

Srinivas Chinamilli

Dear Customer,

Thanks for your continued support to Tessolve. We are continuing to grow and making key investments to strategic areas to be of better value add for you.

We have acquired a PCB fab (Spectrum) located in Johor Bahru in Malaysia. This is a fully operational fab with good capabilities in manufacture of Burn-in, ATE and System/ Reference PCBs. We have offered turnkey PCB design, fab and assembly services for several years now. With this acquisition, we will have better control on fab pricing and cycle times.

We have also acquired a Test Floor in Singapore with turnkey packaging and production capabilities. This is again a fully operational test floor with competent product engineers. They have been offering turnkey packaging and production test services for several customers already. We already have a strong presence in Singapore, with over 150-strong engineering team. This acquisition will further extend our offerings from test and product engineering to turnkey production test services.

On the reliability front, we have added burn-in/HTOL capabilities to our reliability lab. We have two fully operational burn-in ovens that can do chip level as well as system level burn-in. With this, we can enable you to do ESD, Latch-up and HTOL reliability quals right here from our Bangalore lab.

We are also close to making an acquisition in Analog design space. This will strengthen our existing Analog design capabilities. I will give more details on it next time.

We have also started Tessolve, Germany. With this, we can better address your requirement in Germany, Netherlands and other countries in the Schengen regions.

As you all know, **International Test Conference** was held in Bangalore in July 2017. This was truly a historic occasion for having this conference in India for the first time. Tessolve is proud to be a Platinum sponsor for this event. Special thanks to Prasad Mantri, Navin Bishnoy, Triambak, Veerappan and other steering committee members for making this happen, we thank you all for your sponsorships and participation.

Let me take this opportunity for congratulating our employees:

Savinaya for winning the IDIYE competition held by TI in coordination with IEEE Jagadish, C Srini, Sandeep and Gowrishankar for conducting Tutorial and poster sessions at ITC.

Shahsank, Jagan, Karun, Prasad, Shanthanu and team for winning the best poster award at SPARK tech forum held by Qualcomm.

We look forward to providing value add engineering solutions to you and we will work hard to help you in your productization efforts.

Best Regards,
Srinivas Chinamilli

TESSOLVE SHOWCASE

1. Test and Productization Flow for the Next Generation Silicon (IOT)

Jagadish Kumar Chandrasekaran - Director, Srinivasan C - Manager and Gowri Shankar Ilankumaran - Test Engineer

We have presented this Tutorial content in **International Test Conference-2017**, this tutorial was designed for Design & DFT engineers, Test engineers as well as managers who want to get an understanding of the Test and productization flow for the next generation silicon being designed today. The pre-requisite for the Tutorial is knowledge of CMOS chip design and test concepts.

Test & Product Engineering is confronted with the challenges of productization of complex IoTpRoCs (Programmable Radio on Chip) that have a variety of technologies including sensors, low power digital logic and other complex technologies. Test and product engineers are confronted with designing complex test flows while meeting the test quality challenges still keeping the test cost low. Given the economics, market conditions and the complexity of testing pRoCs, Test and Product engineers are required to adopt novel methods to meet the product schedule and cost goals.

The traditional approach of using compartmentalized test methods of sequentially applying digital test, followed by analog test and RF test will not be acceptable test for Internet of Things (IoT) and 5th Generation application scenarios. In order to design, develop and execute the multi-dimensional test procedures, a Test Engineer will have to master test engineering for all the key components of IOT systems including but not limited to High Speed Interfaces and Security protocols, RF subsystem etc.

Our proposed flow comprehended need for ATE debug interfaces and hooks for collecting data for yield engineering while keeping the manufacturing throughput at optimal levels. Tutorial helped participants to get an overview & Evolution of IoT, Low energy consuming architectures, various Test flows for Structural, Functional, HSIO (High Speed Input Output) and RF core testing of IoT.

The Tutorial also addressed the challenges of HSIO and RF test that have a significant role in test and validation of IoTpRoCs. The HSIO topic addressed different types of HSIO test approaches using both Hardware and Software techniques like RAT, Smart loop back, Hard & Soft Synchronization, Internal and External loop back methods. In RF, we discussed how the IoTp RoCs specification fits in the existing ATE instrument available today.

2. Wafer Level Testing: Challenges of using WLCSP Probe Heads

Kamakshy Murugan - Test Engineer, Eashwar Venkateswara Sarma - Test Engineer and Shivaramakrishnan Chandrasekharan - Test Engineer

Introduction to WLCSP Package

Wafer Level Chip Scale Package more commonly known as WLCSP refers to the technology of packaging and using a device directly as a die, instead of the traditional process of dicing individual dies from the wafer and assembling them into final packages. The device's interconnects and protections are accomplished using the traditional fab processes and tools. In its final form the device is a die with an array pattern of bumps or solder-balls with typically 200um pitch. WLCSP technology differs from other ball-grid array (BGA) and laminate-based CSPs in that no bond wires or interposer connections are required.

For a relatively new and much smaller package WLCSP test setups pose new and unique challenges for Test Engineers to overcome. Most of these challenges are related to the WLCSP Probe Head and its arrangement.

Introduction to Probe Heads

Unlike an FT hand socket the WLCSP probe head is not just a mechanical adaptor between the device and the DIB. The probe head consists of 4 basic components. An Interposer, a Fan-out PCB, Cartridge(s) and an SS Frame. Since a die is much smaller than any FT device, the probe head includes a built in fan-out layer.

Cartridges of the probe head are the only component that makes contact with the dies. One cartridge forms contact with one device only. Each cartridge is mounted separately onto the SS frame, from underneath. The cartridges after being mounted on the frame (image shown below) are then attached on to the Fan-out PCB using the corner mounting holes of the SS frame. The signals to and from the device pass through the cartridge and are "fanned – out" by the fan-out PCB before reaching the load board through the interposer. The interposer is nothing more than a link between the Fan-out PCB and the load board.

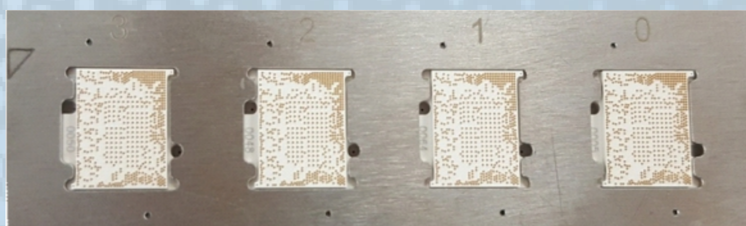

Figure 1: Close up image of cartridges on a quad site probe Head

The Challenge -WLCSP Probing

Proper contact is crucial for a reliable electrical connection. This fundamental requirement must be met to obtain reliable and consistent test measurements. In WLCSP devices the bumps are so minute (in the order of micrometers) that to make proper contact with each bump without shorting with neighboring ones is in itself a great challenge. This touch task is performed by the probe head. Being a very precise activity makes it highly sensitive and susceptible to what is normally considered "negligible" variations and offsets.

We often see that if not perfectly setup the probe head will cause contact related test failures. The following are failures observed when improper contact was found to be the cause; Inconsistent Continuity, Power Short, Few digital tests, LDO tests, TX/RX EVM tests and current measuring tests.

Good contact is essential for proper current flow and hence its absence can cause failures that at first may not seem like a direct consequence of improper contact, leaving the Test Engineer confused and uncertain. While facing such failures, the first suspect must be the Probe Head, provided the Test Head and prober setup are known to be good. Using an offline high resolution 10x – 20 x microscopes the probe head should be examined manually for anomalies. For this kind of debug the Test Engineer must take a patient and organized approach to check and rule out each of the following possibilities step by step.

1. **Overdrive:** Insufficient overdrive is a certain cause of bad contact. Overdrive is how much distance, along the Z-axis, the wafer is pushed up against the probe head. Higher the overdrive, greater the force of contact. The maximum permitted overdrive varies with the type of probe head being employed. However, it is recommended to always follow the OD exercise and base the maximum overdrive on its results. A brief explanation of the OD exercise is as follows.

   While running tests or production in auto probe mode, overdrive must be set to its optimum value to achieve maximum throughput. The OD exercise is a method to find this optimum value. The exercise must start with an overdrive for which all pins fail continuity. It must then be slowly increased in small steps of say 10um, until the first pin passes continuity. This value is taken as OD1. We carry on with the exercise increasing overdrive in steps until all pins pass continuity consistently and across all quadrants of the wafer. This value is OD2. The optimum overdrive to use is given by OD1 + 150um or OD2 + 50um. We generally use the lesser of the two values as the optimum overdrive.

2. **Contamination or Dirt** – Dirt on the cartridge pins is the most common occurrence. This can be resolved by two methods.

   a) Needle Polish – This is a built in feature in most Probers. It uses a mipox sheet to clean the probe head. Parameters such as overdrive and polish count must be set before the needle polish can be performed. Cons; cannot verify visually if the cleaning was effective as intended since it happens internally within the prober.

   b) Manual cleaning – This is the best way to clean contamination by manually examining under the microscope. The additional benefit is that other issues like pin damage/shorts can also be identified. Note that prior training is necessary to perform this task. Only a Horse hair brush must be used for cleaning the cartridge as it is extremely fragile.

3. **Damaged Pin** – A damaged pin on the cartridge will cause consistent continuity or power short failure. The damaged pin must be spotted under the microscope and then mapped back using the ball map to confirm that it is the cause for the failure. The only remedy for this is to change the cartridge. The cause of damage maybe careless handling of the probe head, excessive overdrive or in rare cases a drastic offset in planarity.
4. **Sunken Pin:** A sunken pin is one which has dropped down or sunk in height considerably relative to other pins of the cartridge, such that it is not possible for it to make contact with its corresponding bump on the die. A sunken pin is very hard to spot under a microscope as the microscope's view is directly from above. Each pin in the cartridge must be carefully examined. Tilting the probe head at an angle makes it easier to identify a sunken pin. The concerned cartridge must be replaced to overcome this issue.
5. **Improper mounting:** Site to site variation in results can be caused by improper mounting of the probe head or cartridge.Uneven tightening of screws can cause this issue. One observable side effect will be OD values taken during the OD1 OD2 exercise. The Engineer can notice that certain pins or sites touch down a lot earlier than others or in the worst cases OD2 cannot be determined at all.
6. **Misalignment:** Inconsistent test failures or site to site result variation can also be caused by an alignment offset between the cartridge and the fan-out PCB. The engineer can check this under the microscope as well. If need be the Fan-out PCB can be removed, cleaned and assembled once again making sure the alignment is proper while re-assembling.
7. **Worn out Fan-out PCB:** The Fan-out PCB sometimes gets worn out and if so one can find multiple scratches and in some cases even fine copper dust on the PCB. This may cause power short issues or failures in tests that measure current. The solution is to replace with a new PCB and check the results for verification.
8. **Planarity of Probe Head:** Planarity or flatness of the Probe Head is a major factor that contributes to good/bad contact. Planarity should be checked regularly and must be maintained below spec. It can be checked using the PCI inspection feature in the prober. PCI (multi-point) must be performed every time the test head is docked, a new DIB is placed or whenever the probe head is tweaked.
9. **Pin CRES value:** This is something a Test Engineer cannot measure using an ATE. Even after multiple alignments, cleaning and examining of the probe head, if the same kind of failures persist there is a chance that contact resistance of a few pins has increased or have become unstable. This can be caused by excessive touch downs leading to reduced spring tension in the pin plunger. CRES values can be verified only by sending the Probe Head back to the manufacturer and examining the reports.
10. **Worn Probe Head:** By observing the probe marks of the die bumps and by observing the definition of crown on the cartridge pins, one can come determine if the probe head is worn out or not. This conclusion must be arrived at only after the above steps have been ruled out and if the crowns are visibly and clearly worn out.
11. **Test Head Docking:** Proper docking of the test head is an obvious point to take care off when using a prober setup but sometimes it is prone to being overlooked. The test head planarity after docking is an important factor in the outcome of the PCI readings. It will leave the test engineer working with wrong data. Improper docking can sometimes cause inconsistency in continuity and it may cause TDR to fail as well.
12. **Prober Head Plate Planarity:** The Test Head planarity is directly dependent on the Head plate of the Prober. If the Head plate planarity is out of spec, then not only the PCI readings but test results will also be inconsistent. If a serious doubt arises as to the Head plate Planarity, the prober team must be called in to perform TPG calibration.

Planarity and Its Importance

Planarity is of paramount importance when it comes to direct dock setups. Be it UFlex or 93K systems it is essential for it to be with in spec. In laymen terms, Planarity is nothing but how flat or level a surface is. It is determined by computing the difference in height between the highest point and the lowest point of the surface in question. In this case we are concerned about the Planarity of the Probe Head, more specifically of the cartridges and its pins.

1. **UltraFlex** - While running PCI Inspection in UltraFlex, the prober checks the 4 corner pins of each cartridge measuring the Z value (height) each time and then computing the difference between the highest and lowest pins to give Planarity. This basically tells us which cartridges/pins are higher and which are placed lower with reference to the wafer. It gives us an indication of which sites touch down first and which ones last. Therefore the PCI readings must be co-relatable to the OD exercise data. The site that reads a low Z value must logically touch down first. If Planarity happens to be above spec, for UltraFlex this value is typically 40um, we use the PAB tool to adjust it and bring it down below 40um. In UltraFlex load boards the PAB mechanism is built-in to the RF blocks.
2. **Verigy 93K** – With reference to membrane probe heads used in 93K Direct Dock setups, the PCI readings (measured across 4 points or 16 points depending on the recipe file of the prober) are typically expected to be below 15um. If the readings are out of spec, there is no PAB adjustment mechanism to deal with this like in Ultraflex probe cards. If the PCI readings are more than 25um for instance, prober head plate screws can be adjusted until the readings fall within spec i.e. 15um. Considering the scenario where the readings are will be within spec, but probe marks on the die bumps are weak across a particular site or all sites, planarity screws on the membrane probe head can be tweaked in clockwise or anticlockwise (max of 45 deg/tweak) until healthy probe mark imprints can be seen on the wafer bumps across all sites.

Conclusion

As more and more devices adopt smaller packages like WLCSP and WLBGA, the supporting hardware and engineering for the testing of these devices are bound to improve and become more rugged. Although challenges are being faced regularly by engineers working with WLCSP related hardware, these issues are being overcome constantly and WLCSP devices are running very successfully in production with high outputs. Issues are bound to arise. The goal is to comprehend the underlying issues and formulate reasonable solution steps and debug procedures.

3. Script approach to test the multimedia device

Nagendra Bankupalli - Team Lead

Introduction

The System is HD media server supports playback media content up to 4K and can stream the Full-HD content via Ethernet including surround audio.

System overview

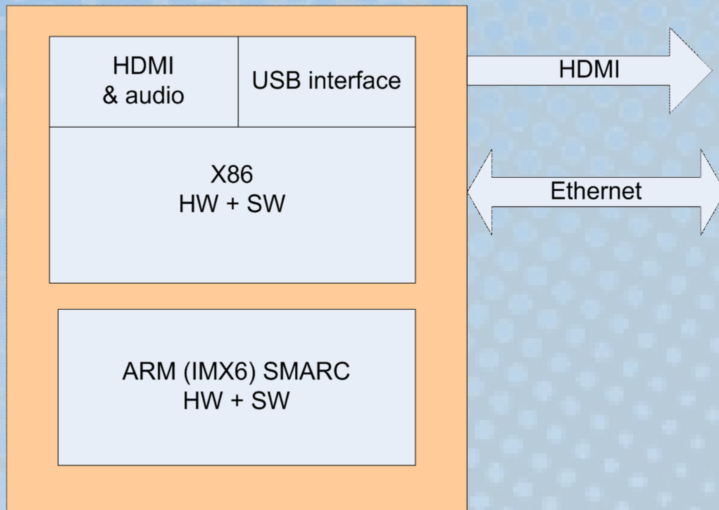

Figure 2: System Overview

Main Features

1. Media Playback from USB, SD card, DVD and CD
2. Supports 4K output and 4K media playback
3. Dual Display (4K + Full HD : 1080i60/1080p30/1080p24/1080p60/1080i50)
4. Full-HD video streaming with Surround Audio (MPEG-TS/RTP-SDP)
5. Supports Chrome to display web content
6. As there are many feature and components in the system , it needs many commands to control them like Player control, System control, Stream and GUI control etc.,

Complexity of the System

1. As the system is a media device, it has complex architecture and blocks, each block controlled by its own set of commands, the blocks would be like,
   a) System
   b) Media
   c) GUI and streaming
2. The system commands basically control overall system like
   a) Display
   b) Resolutions
   c) Temperature reading
   d) Network control
   e) Fan control
   f) Software update and version control
   g) Error log report
3. The media commands basically control media playback and media control like
   a) Disc info and playback
   b) USB info and playback
   c) Multiple instances of playback
   d) Volume control
   e) Language subtitle control
   f) Pause, start, stop, mute and menu control.
4. The GUI and streaming commands basically control streaming and GUI display
   a) GUI open, close, CONFIG URL.
   b) Stream video control.
   c) Stream audio control.
   d) Stream format control (MPEG-TS/RTP).
   e) Stream Ethernet port and address configurations.

Nature of the challenges

1. Writing test applications with these combinations of various commands are time consuming and bottle neck for testing such complex system.

   For example, to configure the system, the following commands are used.

   TES_VIDEO_HDMI1_STATUS

   TES_SET_DISPLAY_MODE

   TES_VIDEO_HDMI2_STATUS

   TES_VIDEO_HDMI1_RES_SET

   TES_VIDEO_HDMI2_RES_SET

   TES_AUDIO_VOLUME_INITIAL

   TES_FAN_INIT_POWER_SET

   TES_NETWORK_SET

   TES_NETWORK_MODE

   Each command need specific argument and to be called in various sequences to achieve required configuration. Like this the system has other media-player and streaming commands.

   MP_OPEN

   MP_TES_PLAY

   MP_BRING_PLAYER_FRONT

   MP_TES_UP

   MP_TES_RIGHT

   MP_TES_ENTER

   MP_TES_DOWN

   MP_TES_AUDIO_VOLUME_INIT_SET

   MP_TES_AUDIO_VOLUME_UNMUTE

   MP_TES_PLAYBACK_SPEED

TES_SET_STREAM1_RESOLUTION

TES_SET_STREAM1_PORT_NUM

TES_SET_STREAM1_DESTINATION_IP

TES_STREAM_START

2. Requirement is to test and validate
   a) Each individual command
   b) Each block of the system
   c) Functionality of the system like playing from USB, disc and streaming.

3. Challenge is to write test application with various combinations to achieve above requirements, which leads us to complications like
   a) One SW resource should be dedicated to write applications in C.
   b) Compile them every time, with changing arguments, sequences as required.
   c) Any minor change in application or command, the SW should get recompile again.

The Script Approach

To address above challenges Script approach has chosen. The advantages are,

1. This approach does not require a SW guy writing all test applications as all scripts are written in simple Text file.
2. The script is combination of commands that anyone can create (one should know the commands).
3. No compilation, as script is written in Notepad, parsed and executed by main application.
4. Only single application is sufficient to run multiple scripts.
5. No more writing application, create text file with required commands in order.
6. Even HW people can create their own sequence to test a specific scenario without any help.
7. The scripts are flexible to alter "any command, any arguments, any sequence" on the spot which leads to better testing (no need to wait for recompilation and re-writing test application).

Example Script

Below is example script with combination of system, media and stream commands.

```
#------------------------------------------------------------
#       Set Extended mode
#------------------------------------------------------------
TES_GET_SOFTWARE_REV
USR_CMD
MP_GET_VOLUME_NAME_DVD
USR_CMD
TES_SET_DISPLAY_MODE     TES_DISPLAY_TES_2X
USR_CMD
TES_X86_APP_RESTART      TES_APP_TES_1
TES_SLEEP                3
TES_X86_APP_RESTART      TES_APP_TES_2
TES_SLEEP                3
TES_X86_APP_RESTART      TES_APP_TES_CLONE
TES_SLEEP                3
USR_CMD
#------------------------------------------------------------
#       Check for HDMI1 and 2 changes
#------------------------------------------------------------
TES_VIDEO_HDMI1_RES_SET     TES_PLAYER_HDMI1_2160P_24
TES_SLEEP                   2
#
#
TES_VIDEO_HDMI2_STATUS      TES_BOTH
TES_SLEEP                   2
#
#------------------------------------------------------------
#       Check dvd play on hdmi 2
#------------------------------------------------------------
MP_OPEN                          TES_PLAYER_2
TES_SLEEP                        2
MP_TES_PLAY                      TES_NO_DVD_MENU
USR_CMD
MP_BRING_PLAYER_FRONT
USR_CMD
#------------------------------------------------------------
#       stream1 1080p30
#------------------------------------------------------------
TES_SET_STREAM1_RESOLUTION          TES_STREAM_1080P
TES_SET_STREAM1_AUDIO               TES_STREAM_AUD_SIX
TES_SET_STREAM1_PORT_NUM            5080
TES_SET_STREAM1_DESTINATION_IP      172.17.255.255
TES_STREAM_START                    TES_STREAM1
#------------------------------------------------------------
##
```

Figure 3: Example Script

Conclusion

This specific script approach is helped in removing overhead of writing various test applications which helped in saving time and made testing flexible and easy.

TESSOLVE ENGINEERING CHALLENGE CONTEST

1. Modem Test assembly for mobile chip Testing

Ashwini Deshmukh - Manager, Thirukumaran Dechinamoorthy - Sr. Design Engineer

Purpose of this platform

The purpose of modem test assembly is to test full functionality of mobile chipsets for various customers in diverse geographic locations with specific RF requirements. This enables our client to demonstrate to their customers that these chipsets meet the designed/high level performance standards when assembled into a representative form factor using standard techniques similar to typical commercial handset design. Data is gathered and presented to support this requirement. As a test platform, it allows for verification and validation of a complete mobile chipset.

Modem Test Assembly Specification

This version of modem test assembly is 4G compatible and supports a 5.5" QHD display, Dual flash 22MP rear camera, Dual Front Camera, 6GB RAM with 64GB internal storage, NFC, USB- Type C with Wi-power charging.

Figure 4: 3D Model

Design Challenge

Mechanical design was approached with common footprint design for two different chipsets to enable reusability of plastics thus benefitting from a cost and schedule perspective. Due to the need to accommodate different modules based on different customer requirements in a single phone housing and testing functionality being more critical than aesthetics, these modem test assemblies are bigger than commercial phones.

This phone is designed with modular approach to facilitate easy swapping/access of typical parts such as Rear camera, battery, RF port access etc. Hence an easily removable camera door, battery door, RF plug etc have been incorporated in the mechanical design. Most of the mechanical parts are injection molded plastic parts. All the peripheral components locations (USB, SD card, Audio jack, power and volume button....etc) are fixed on BB (Main) CCA considering best possible ergonomic position in conjunction with chipset layout floor plan. This phone was designed to meet strict grounding/ radiated requirements on par with commercial phones. This included designing new shields and grounding mechanism for EMI shielding. Detailed interconnection document was prepared for various RF antenna sharing configurations.

2. Engineering ATE Usage Time Reduction for RF devices

Jagadish Kumar Chandrasekaran - Director, Srinivasan C - Manager, Sandeep Bishamber Singh - Test Engineer and Gowri Shankar Ilankumaran - Test Engineer

Abstract

This article will describe the test strategy for the ATE Test Engineers to reduce the Engineering ATE usage Time (NRE Cost) by two key approaches,

1. The novel DUT load board design having the compatibility with both ATE and the Bench setup by adding more exhaustive provisions in the load board.
2. Enhancing the utilization of the offline tester mode to reduce the ATE usage time by,

   a. Generating the expected DUT output using device models and feeding to test routines for its functionality.

   b) Capturing the raw DUT output and feeding them for analyzing/optimizing the test algorithms.

Scope

Nowadays, ATE usage time is the one of the key factors to meet Time to Market goals and NRE cost. Specifically for RF devices it becomes more important to reduce engineering cost and time due to following reasons.

1. Testing of RF devices consume more Engineering development and debug time due to the complexity involved.
2. Usage of ATE with RF capability on hourly basis is very expensive compared to other ATE configuration.

Engineering ATE Usage Time is the time taken for Load Board Bring up,new instrument routines Bring up, DSP routines Validation, Test Debug and Time for Device Characterization, Test Time Optimization, Yield Optimization, Data collection and GRR.

Factors affecting the Engineering ATE Usage Time

The mismatch or test failure can be caused because of several attributes like test program, setup issue, load board behavior or silicon behavior, etc. Identifying the root cause for the failure or mismatch is difficult in such situation. It may take significant amount of Tester and debug time to understand/differentiate the issue.

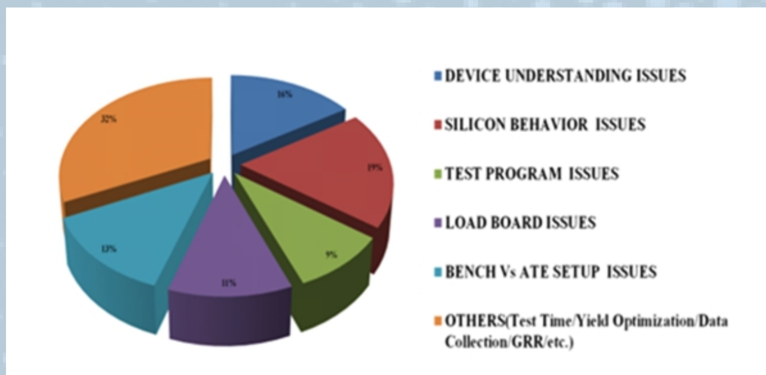

Figure 4: Factors Affecting the Engineering ATE Usage Time

Solutions to problem statement

1. Following the novel test flow
2. Load board design consideration
3. Keen care in test program development
4. Provisions in Load board for debug

Advantages

1. Minimize ATE usage time in turn the NRE cost.
2. Reduction in debug time, hence Time to Market.
3. Simultaneous verification in ATE & Bench leads to reduced total bring up time.
4. DSP routines validation in pre-silicon stage.
5. Eliminate variables like device understanding, silicon behavior, test methodology and load board issues without consuming ATE usage time.
6. Helps to narrow down Bench vs. ATE correlation issues and avoid system return.
7. Reduces the involvement of Designer in ATE environment.

Conclusion

This methodology requires efforts on designing a load board that will work on ATE as well as Bench, but the saving of engineering ATE usage time justifies the additional efforts in designing ATE load board. The additional advantage of using this methodology is that the Bench setup will minimize ATE to Bench correlation effort. This will also help system return and test coverage improvements as the results from system test failures can be mapped back to the ATE environment to improve production test quality.

The statistics explore how much aggregate has been reduced in ATE usage time over various factors in RFID project.

Improvisation

Apart from RF devices, we are looking to implement thismethodology for High speed, PMIC and other Analog devices.

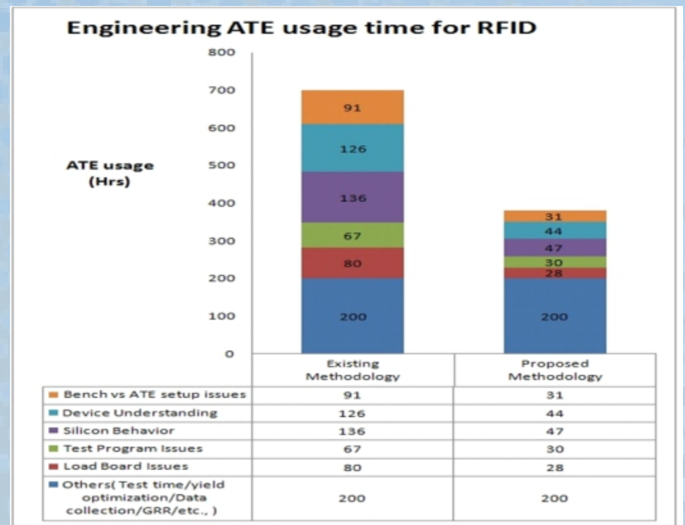

Figure 5: Engineering ATE Usage Time for RFID

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