FIRST BIN

A newsletter for the semiconductor engineering community

TESSOLVE
Delivering Excellence in Semiconductor Engineering

From The President's Desk
Srinivas Chinamilli

Dear Customer,

We are poised to achieve a >30% growth this financial year. Thanks for your support!

We are continuing to invest in growth and continuing to expand in adjacent areas to provide better value adds for your engineering needs. We have added over 400 engineers in the last 12 months. We have expanded our offerings to Post Silicon Validation as well. We are also augmenting our Reliability test equipment with two new burn-in ovens that will address both chip level HTOL as well as system level burn-in tests. With these offerings we have further strengthened our capability to offer end to end engineering solutions for silicon productization.

As you are aware we had officially started Tessolve Malaysia last year and we have ramped up to 50+ engineers in Penang and other cities. We are looking at doubling the engineering presence in Malaysia in the next 12 months. This is a good addition to our already existing 150+ member team in Singapore. This has further enhanced our capability to support design, test and product engineering initiatives out of Asia.

Our integration with Hero Electronix has been completed. It has been a very smooth and seamless transition. Tessolve will continue to be an independent entity under Hero Electronix umbrella. Hero's commitment to further investments in electronics initiatives aligns very well with Tessolve's passion to expand semiconductor productization eco system in India and other parts of the world. Let me take this opportunity to congratulate our Lab Team at TI who have been recognized with an award at the Site Meeting for handling over 17000 tickets with 100% positive lab user feedback.

Tessolve was a platinum sponsor for India Electronics & Semiconductor Association (IESA) conference in Bengaluru this year. We had showcased our various product and solution offerings at the conference. It was a very successful event and we could meet several of our existing and prospective customers and have productive discussions.

Best Regards,
Srinivas Chinamilli

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Effect of Mechanical Boundaries on RF Devices and Need of 3D Simulation

Siva Pavan Anala - Sr. Test Engineer

Effect of Mechanical Boundaries on Performance of RF Devices

Introduction

This document highlights the limitation of ATE for RF devices like Power Amplifiers & back to back driver amplifiers testing.

Limitation

- Limitation of Active IC's and its associated components in handler layer.
- Test engineer does not have enough command over mechanical constraints.

Cause of oscillations andiInstability due to cavity resonance

- The effect of cavity resonance is mainly due to the module height and the housing structure.
- The standing wave has the characteristic such that the E and H fields are 90° out of phase with each other.
- The impedance will therefore fluctuate wildly across the cavity causing unknown effects on circuitry including the introduction of instability to active devices.

Recommendations for PCB

- Walls in the PCB to avoid cavity resonance.

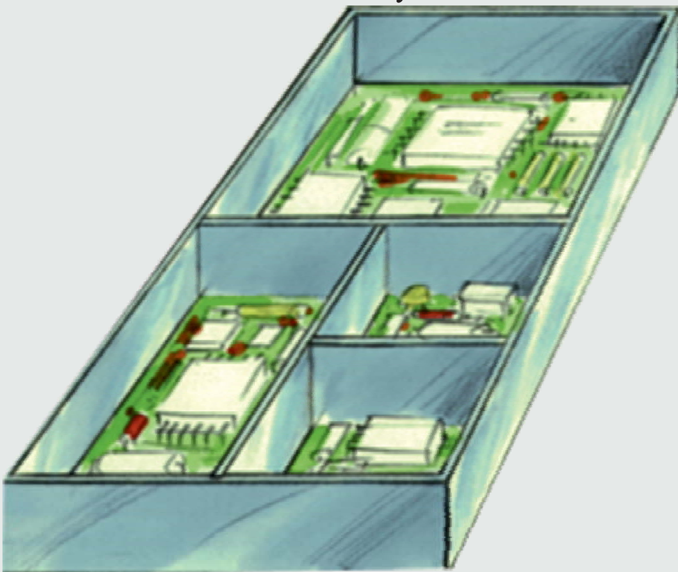


Figure 1: Walls in the fixture

- Additional space around the structure.

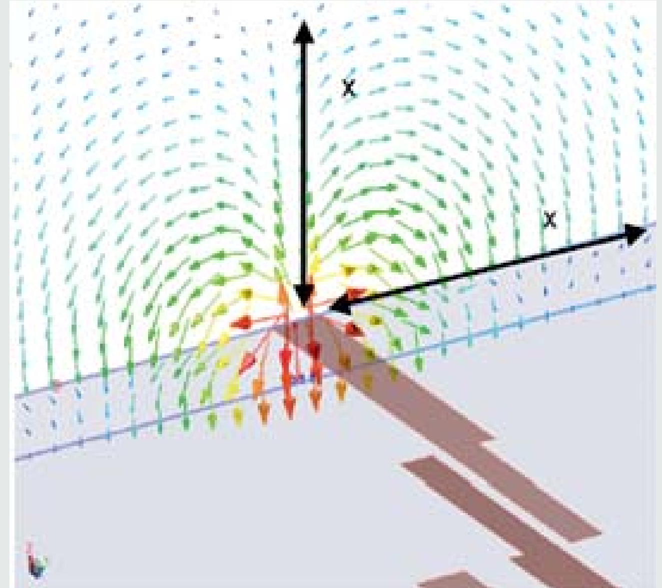


Figure 2: For Microstrip Design - Rule of thumb

- Distance from Open boundary
  - Lateral >5 line widths
  - Vertical>5-10 substrate heights

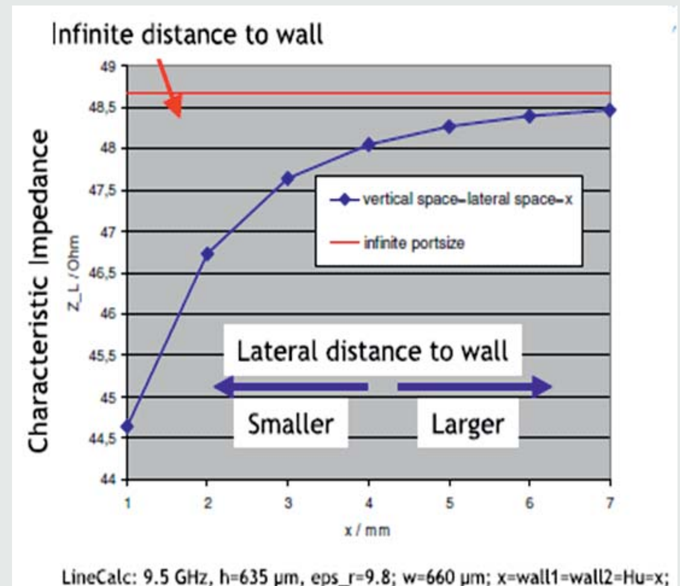


Figure 3: Effect of impedance WRT to distance to the wall

Need of 3D (FEM/MOM) Analysis in RF Board

Introduction

Simulation is needed for the computation as RF field probe measures E & H plane. Manual computation is impossible as RF deals with Maxwell equations.

Types of simulator

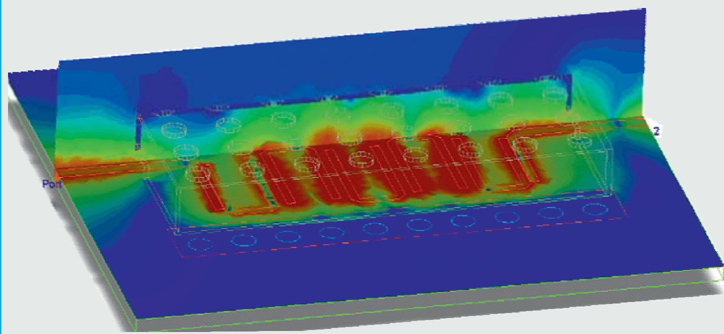


Figure 4: 3D Electro Magnetic Simulation

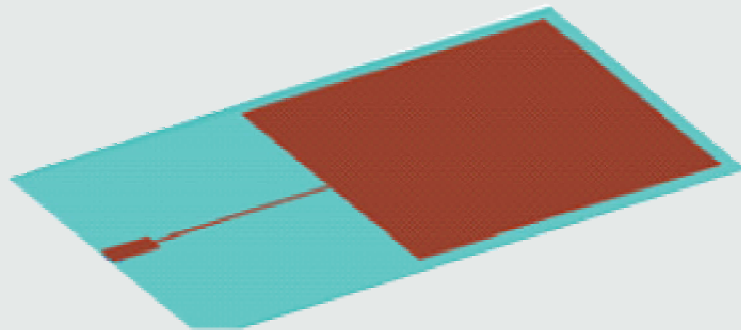


Figure 7: Patch Antenna

There are three different types of simulator

1. Circuit theory based simulator

Analytic model determines input & output behavior of components.

- Advantages : Fast Results.
- Disadvantages : Not accurate and real time but close to actual response.

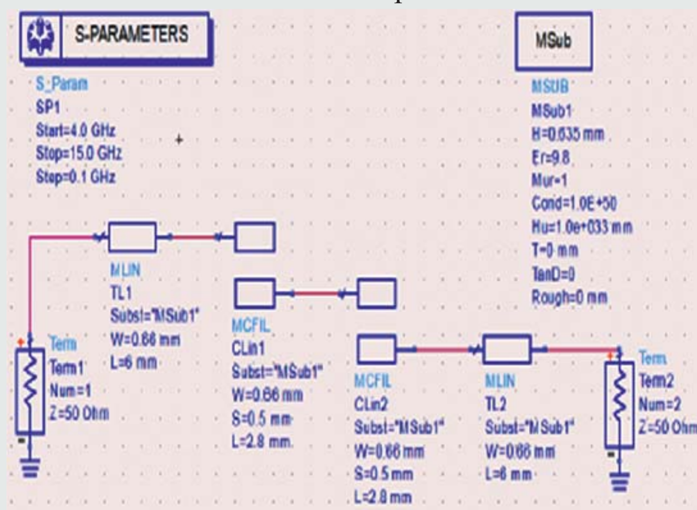


Figure 5: Circuit based simulator

2. Method of Moment (Mom)

- Full wave solver for layered media, arbitrary planar geometry.
- Arbitrary 2D metallic structures and vias in layered media
- Substrates are infinite in lateral direction
- Mom is applicable for multilayer designs, Planar Antennas and to visualize the current density

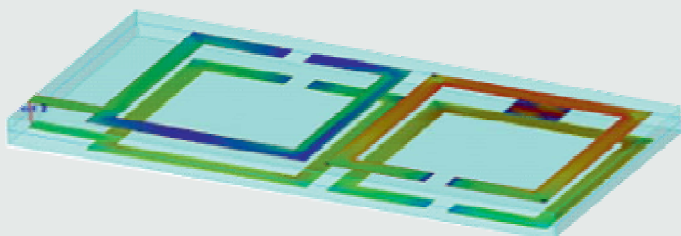


Figure 6: Multilayer Designs

- In Mom mesh quality is crucial, basically mesh is for subdivide metallic strips in basic 2D cells and each cell size is bases on cells/wavelength.
- There are different edge meshes.

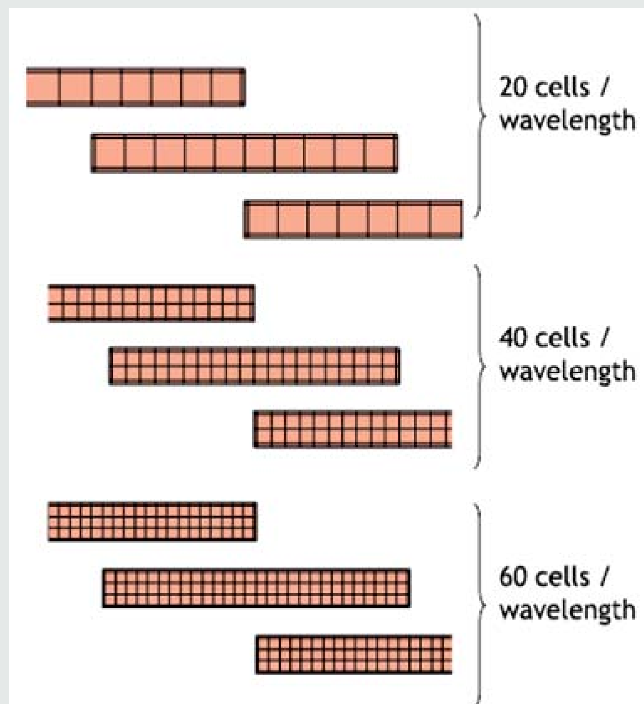


Figure 8: Different Edge meshes (central section of edge coupled line filter)

3. FEM (Finite Element Method) Analysis

- Mom is 2.5D whereas FEM is real 3D simulator.
- Substrates are finite in lateral direction.
- FEM is applicable for multilayer designs, connectors to visualize the E,H distribution.

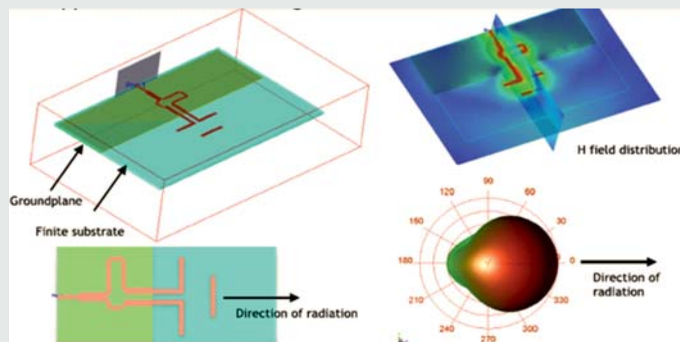


Figure 9: Radiation in FEM

ATE Board Design Challenges for 0.35mm Pitch Device Involving Wireless & RF 5G Signals

Selvaraj S - Sr. PCB Design Engineer

Scope of work

This case study describes the PCB Layout design consideration and challenges while designing boards with RF5G, RF2G signals and blue tooth wireless technology. This project is an octal site WLCSP Probe card (0.35mm pitch DUT) designed on a 46 layers Multi-lamination stack up.

Problem Description

Layout design for this project was very complex as there were several restrictions to use power and digital channels from tester. The device being a wireless chip posed extra challenges in placement and routing of the RF circuits. Arriving at a stack up, that is manufacturable, to meet these requirements was challenging. We ended up with a 46 layer Multi-lamination stack up that had back-drilling (stub removal) requirement for the RF DUT at 0.35mm pitch.

Challenges Encountered during RF Placement

- Both RF 5G and 2G circuit's placement was done by considering many parameters such as Signal propagation delay to be same across sites, arc routing is required to make smooth transmission line and need to control the cross talk issues.
- RF 5G signals (Band width is 20MHz) were routed at micro strip line environmental which works at 5Ghz of operating frequency and 25dbm maximum power.
- 2G signals were routed in Signal1 (Layer 3) which works at 2GHz operating frequency. Also, the back drilling (stub removal) process was done specially for 2G DUT vias in order to control the signal reflection. Please refer Fig. 1.
- These RF signals are generated from external source. It is given to DUT through RF switch and DUT output is also measured through same RF connector (for 5G, 2G and Blue Tooth). Those are controlled by SP4T RF switch which can work up to 8 GHz. This bi directional operation is basically called as Vector Signal Analyzer or VST.
- GND stitching (Coplanar wave guide – CPW) is used around the RF signals to avoid the cross talk issues. Both partial and through hole via were used for RF ground shielding purpose. Partial GND via will be present only from Layer 1(Top) to Layer 26 (book1 lamination).

Risk factors in the design execution

5G signals were routed at micro-strip line environmental without adding delay tune. Usually length match is done by adding delays in the routing but in this design, RF components were tuned in order to obtain the same length across site..

- The fig. 1 shows the RF 5G signals routing and it looks to be NOT length matched as there is no delay tune but, length match has been done across site by tuning the RF circuits placement accordingly.
- 2G signals were routed at Strip line environment and trace length was matched by tuning the RF components as said above to obtain same propagation delay for each site. Please refer Fig. 2.
- Also back-drilling (stub drill) process was used to remove the unwanted stub for 2G signal vias at the DUT. Stub from Layer 26 to Layer 4 was removed.
- Note: Layer1-Layer 26 is the first book in the stack up and Layer 27 to Layer 46 is the second.
- Back drilling process was very complex for fab vendor to do for 5 mil drill via in a 0.35 mm pitch area.
- Power (Copper) plane has been used for WL_VDDC and BT_VDDC power domain. Ground plane is surrounded around each power domain in order to isolate from each other and control the unwanted noise or coupling in book1 lamination.
- Remaining power domains have been routed with 50mil trace width, 8mil trace width (Measurement signals only) and covered with copper plane in book2 lamination. Each power is surrounded with gnd and isolated from each other.

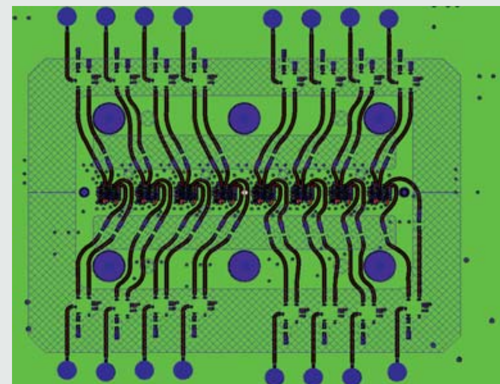


Fig. 1: 5G RF in & out signals routed at DUT side – With CPW

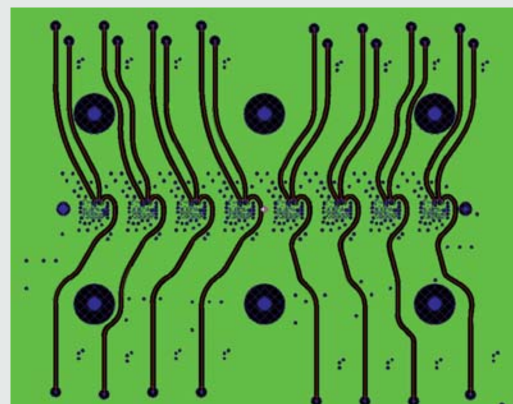


Fig. 2: 2G RF in & out signals routed at signal1 – With CPW

High current Power domain channel restriction

Each power domain was assigned to tester resource with below consideration.

- UVS256 can run with -2V to 18V also can support up to max 800mA load in high current mode but in standard current mode UVS256 can support up to max 400mA load only. Few power domains required to have high current mode so we assigned the channels as n to n+3 (where n = 1, 5, 9, and so on) to the same DUT (to run at high current mode as per tester mandatory) because groups of four channels share the same DGS signal.
- UVI80 can run with -2 to +7V also can support up to max 1A load per channel. Totally 80 channels are available and it was sliced into 10 bit modulo (1-10, 21-30, 31-40, 41-50, 51-60, 61-70, 71-80) and assigned for each site. All sense lines were tied at DUT pins only. All layers were required to have GND flood around each power plane, routing and digital routing for better copper balancing and to eliminate crosstalk.

Stack up complexity

- This design was built with 46 layers stack up and to 235 ±10 mils thickness.
- This design had two laminations. Book1 was fabricated with 26 layers and able to meet 50 ohm impedance requirements. Book1 thickness is 90 mils.
- Two different di electric materials have been used in this design (Megtron 6 & Isola 408HR) which is called as hybrid stack up.

Conclusion

This design had lots of challenges while placing the components, routing critical signals, laying out PWR/GND planes and achieving signal impedance with such a high layer stack up. This design had 14 signal, 10 power and 4 different ground layers. This kind of design was already executed at customer end for 6X & 11X projects but, there were issues in Site to Site correlation. This 8X project was fabricated and assembled successfully and the Site to Site correlation met the requirements. This design can be used as reference for upcoming RF 5G projects.

Yield Improvement by Redundancy Implementation

Sajin.K - Test Lead & Arjun Gupta - Test Engineer

The term redundancy refers to the incorporation of redundant circuitry in a section of hardware that is more prone to yield errors. The redundant hardware being part of the full design makes it more complex and the testing of the same becomes far more challenging.

In this particular project, the device under test (Image Sensor) has processing circuitry redundancy where the processing path of the device embeds a full redundant slice. A slice block contains PGAs, ADCs, WAM & MAC processor and a serializer. The connection of the redundant block is programmed via SPI interface by utilizing redundant slice and ignoring defective slice.

Device Redundancy Description

The device consists of 16 slices (0-15) of processing blocks between Serialization block and framing block. There is one redundant slice present for 16 slices.

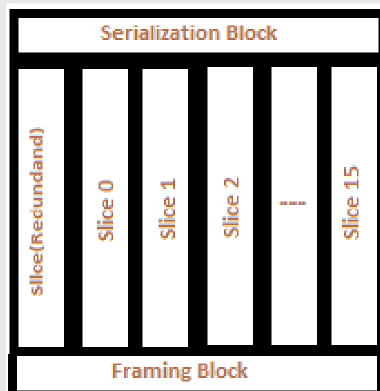


Fig1. Image with redundant processing circuitry.

The redundant slice gets enabled if any one of the slices from 0-15 fails due to hardware issues.

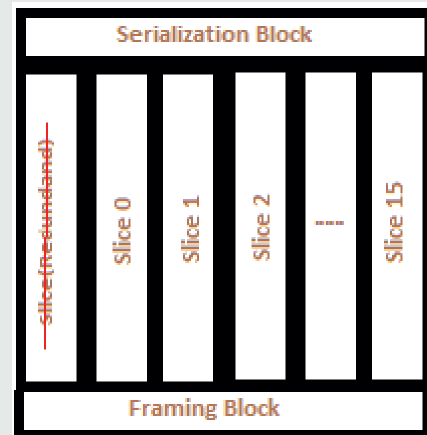


Fig2. No slice failure

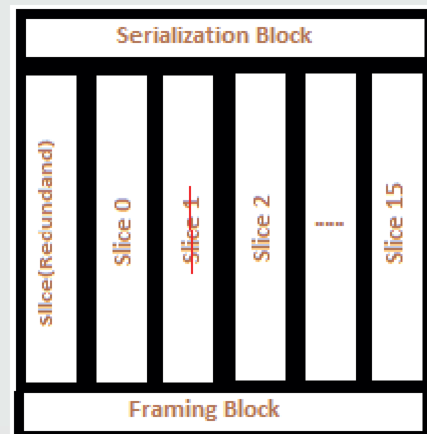


Fig3. Using redundant slice for failed slice

Redundancy Test Algorithm

1. Capture the Test Image from the sensor (Raw data from 16 slices).
2. Execute Image processing library function to check slice failure using image comparison method.
3. Check for failure and it will return one of the following values.
   - a. Value 77777 : If there is more than one defect within the slices.
   - b. Value 88888: If no defects found and redundancy is not required.
   - c. Array_Index: If only one slice defect is found, it will return the corresponding slice number.
4. If return value in step 3 is 77777 or 88888 skip the following steps and go to Step 7.
5. Execute the redundancy correction function by modifying the registers used for selecting the redundant channel.
   - a. Identify the failure slice from the step 3.
   - b. Set the redundancy mux channel according to the failure slice using on the fly pattern changing method.
6. Execute Step 1, 2 and 3 using modified Pattern.
7. Check for the return value
   - a. Log the results as pass if the return value is 88888.
   - b. Log the results as fail if the return value is 77777 or other values.

Redundancy Test challenge

1. Slice Redundancy Algorithm.
   - a. The data sent by the device has to be arranged in a specific format by rearranging the image to contain 16 column.
   - b. ns and each column should represent the respective slices.
   - c. The rearranged image is then compared with golden image to create defective map which shows the defects in the image. The defective map will have the same size as that of the rearranged image but will contain the values of 1 and .
   - d. Find the total number of defects in each column and compare it with threshold value.
   - e. If the number of defects in each column is higher than threshold values, then the corresponding slice is considered as faulty.
   - f. The threshold will be selected based on the maximum expected pixel defects and it should be greater than the number of expected pixel failures. This will separate the slice failure from the pixel failure.
2. Readout Channel Redundancy Algorithm:
   - a. Detection of Readout channel failure:
     - I. Capture the Half scale images which has the high probability to find the redundancy.
     - II. There are 2560 readout channels in the captured image and they are divided into 32 groups.
     - III. Each of the 32 groups has 80 readout channels/columns and each group has 1 redundancy channel.
     - V. Take the 80 columns x 832 rows of the first group.
     - VI. Create a defective pixel map using upper and lower threshold or by polyfit methods. Calculate the total defective pixels column wise and compare it with the threshold.
     - VII. If any of the columns are defective, it indicates the readout failure for that particular readout channel.
     - VIII. Repeat the above steps (v to vii) for the remaining 32 groups.
     - IX. After step viii, the function will return the failed readout channel number for 32 groups.
     - X. If there is more than one readout channel failure in a group, then the redundancy will not be applicable and the device will be considered as faulty.
   - b. Readout channel correction using redundancy:
     - I. Based on the failure readout channel, create the Enable or disable array bit stream for ADC channel and MUX.
     - II. The array would contain 1's and 0's to enable or disable the redundancy.
     - III. The array data will be uploaded to the sensor using SPI protocol and only 8 bit can be uploaded at a time using on the fly pattern change.
     - IV. Due to 8 bit limitation, we need to program the sensor 335 times for MUX and 340 times for ADC to cover all the readout channels.
     - V. Once the redundancy is enabled using above steps, capture the image and verify the image to be fine.
     - VI. The above method of 8 bit uploading of all the values will lead to more test time. To reduce the test time, we had come up with the comparison method.
     - VII. In the comparison method, we compare the actual 8 bit data with the golden 8 bit data for all readout channels.
     - VIII. The sensor will be programmed only with data that are different from golden data. This reduces the test time significantly.
3. Created simulated failure environment to verify the redundancy as we did not have any device with redundancy failures. In order to validate our approach, we had to simulate the failure slices from the good DUT by disabling one of the slices.

JTAG Protocol via Flex Rio FPGA

Veeranna Babu I - Test Engineer

Scope of Work

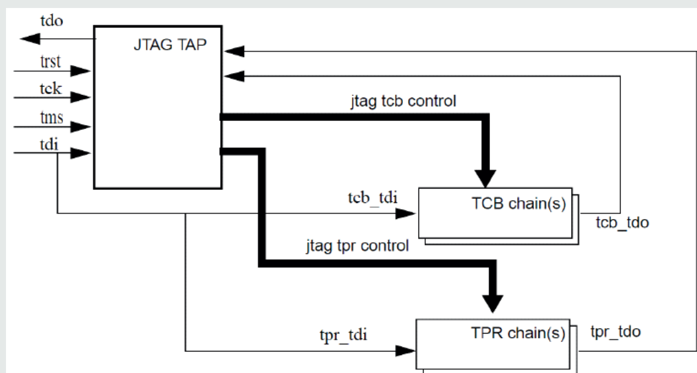
This document describes the flow to access devices for boundary-scan via JTAG (Joint Test Action Group). Generally JTAG is a debug interface where scripts will be developed by a DFT engineer in ATE systems. To make use of these ATE scripts in Bench environment we have implemented the JTAG interface protocol in FPGA of PXIe hardware in LabVIEW environment.

Here, JTAG is used for writing data to the system and reading data from the system memory while testing devices in an automated test environment. National Instruments PXIe chassis (1085) & NI PXIe-8880 Embedded Controller containing NI-6583 (for DIOs) and NI-7962R FlexRIO (FPGA Vertex-II) is the hardware setup for automation purposes. LabVIEW is used to develop the software environment to interact with the PXIe chassis as well as the DUT board.

Challenges

- Synchronizing PXIe clock with DUT clock and other Bench equipment.
- Development of JTAG protocol within the FlexRIO in LabVIEW environment.

JTAG Architecture



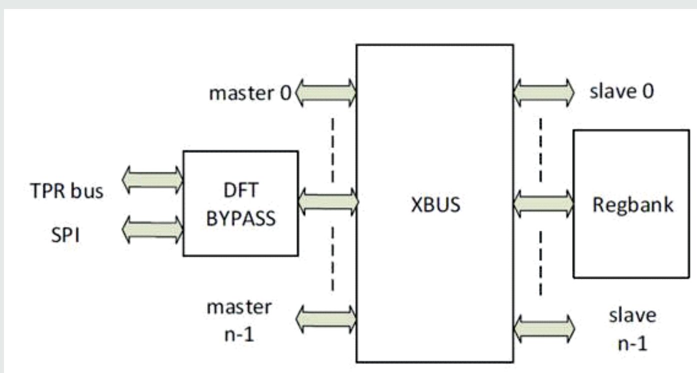


Fig. 1.0: LabVIEW Implementation

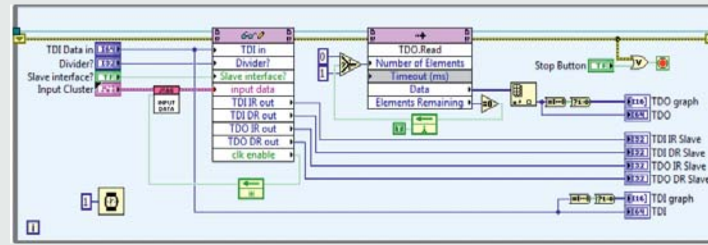


Fig. 2.0: Top Level VI of the host

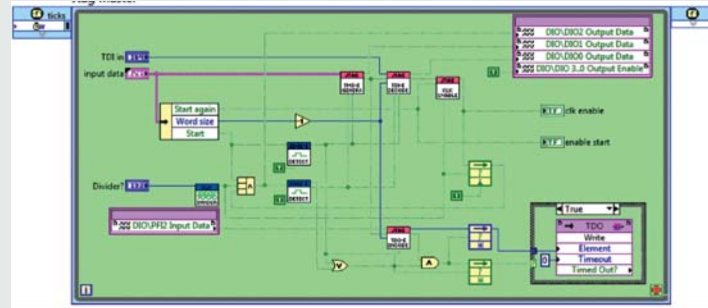


Fig. 3.0: Top Level VI of the FPGA Master Device

JTAG is implemented in LabVIEW in two parts

- The first is the Host VI "JTAG Host.vi," and the second is the VI on the FPGA "JTAG FPGA.vi." The host sends in the TDI control signals to the FPGA.
- The FPGA takes these inputs and performs two different operations, depending on the control (TMS) signals given.
- The FPGA could either send or receive the TDI/TMS/TCK/TDO data to a physical JTAG device.
- The host (Fig2.0) sends to the FPGA, and the FPGA (Fig 3.0) receives from the host vice versa the following:
  1. TDI Data in – this control is the TDI data. It can either be an instruction or data type, and must be specified by the user.
  2. Divider? – This control determines the TCK frequency. The frequency is calculated as follows: TCK = 40MHz/(Divider?+1)*2. If divider value of 0 is valid, and will give us a TCK of 20 MHZ.
  3. TDO – the output data that comes from the JTAG device and to Host Vi through FIFO.

Conclusion

With this approach, ATE scripts generated by DFT can be utilized to validate the bench systems. We can tap the internal circuits for debug by these scripts and it would be impossible if we use the routine SPI protocol.

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