

# THE QUEST FOR BUGS

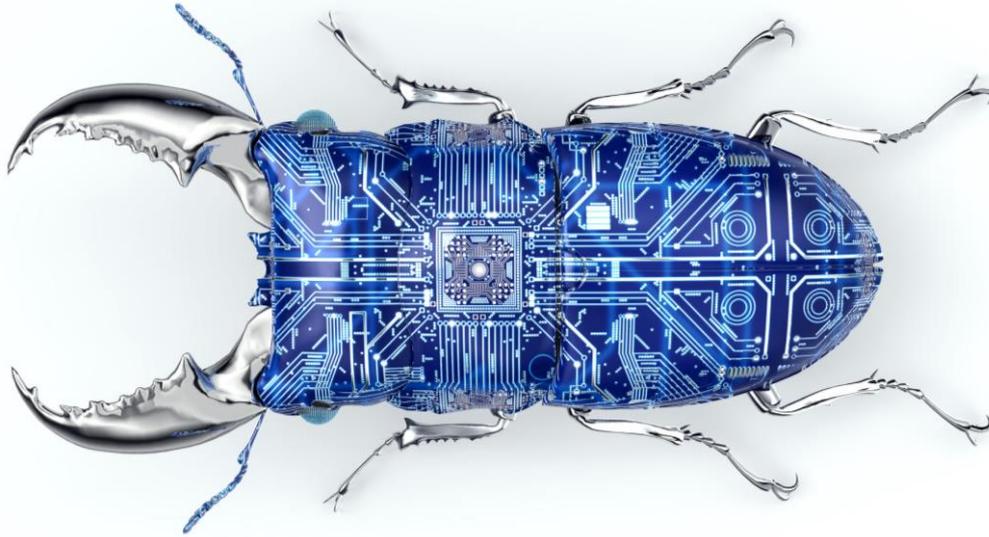
A Bugs Orientated Approach to IP Development

**Verification Futures 2022**

Bryan Dickman, Valytic Consulting Ltd.

Joe Convey, Acuerdo Ltd.

# A Bug focused approach... (understanding Bugs)



ASIC Hardware Verification is a resource limited **'quest'** to find as many bugs as possible before shipping.

*It's a long, difficult and costly search; constrained by cost, time and quality.*

# Who are we?

## Valytic Consulting Ltd.

Verification

Engineering Leadership

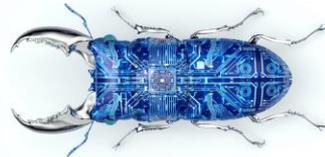
Analytics

**Bryan Dickman**

bryan.dickman@valytic.co.uk



**Collaboration to offer**  
Verification expertise  
Capability Baselineing  
Transformation Strategies  
Thought leadership (QfB)  
Technical guidance  
Senior team advisory  
Marketing



See <https://www.acuerdo.co.uk/thequestforbugs>

## Acuerdo Ltd.

Engineering Platform (EDA)

Strategy and Commercial

Technical Marketing

**Joe Convey**

joe.convey@acuerdo.co.uk



# Verification Technology is Cool ....

- We work in such an intellectually stimulating area of industry
  - Dealing with challenges of building and delivering multi-billion gate ASICs designs and highly complex IP products
  - Where the EDA industry has led the development of some fantastic IC design tooling and methodologies
  - And IC designers are constantly looking for ways to be more effective
    - Deliver faster, at lower cost, with higher quality!
- But....
  - Don't lose sight of the problem.
    - HOW TO **FIND** BUGS!
    - HOW TO **AVOID** BUGS!

# THE DILEMMAS OF VERIFICATION

1. "The Completeness Dilemma"
2. "The Complexity Dilemma"
3. "The Constrained-Random Dilemma"
4. "The Resources Dilemma"
5. "The Delivery Dilemma"



# THE ORIGIN OF BUGS

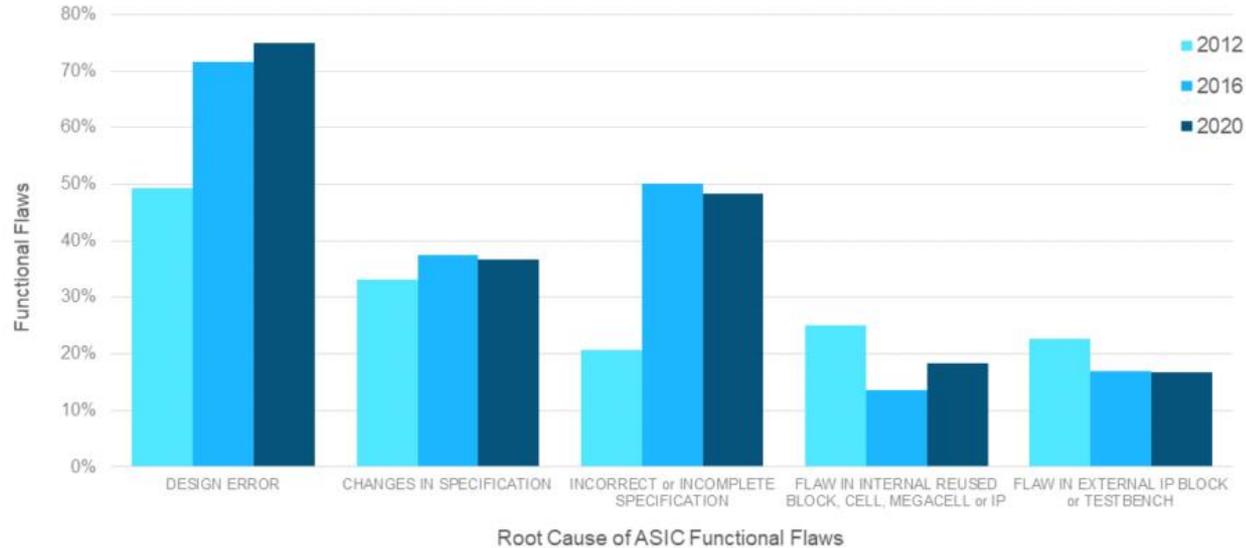
*Where do bugs come from?*

*What are the common ways that bugs are introduced into designs?*

*What can design engineers and verification engineers jointly do to avoid them?*

# Where do Bugs come from?

## Root Cause of ASIC Functional Flaws



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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Figure 12-5. Root Cause of Functional Flaws

<https://blogs.sw.siemens.com/verificationhorizons/2020/10/27/prologue-the-2020-wilson-research-group-functional-verification-study/>

# Functional Bugs and other Defects

- Think of Bugs in the following terms:
  - Functional Bugs
  - Performance Bugs
  - Power Bugs
  - Security Vulnerabilities
  - Functional Safety Integrity
  - Architecture/Specification Bugs
  - Implementation Bugs

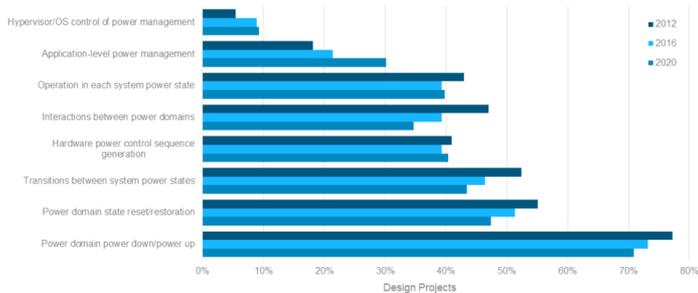


# Power Bugs



- Power Bugs can be catastrophic!
  - Power Intent bugs
  - Failure to meet power budgets
  - Power consumption corner cases presented under real-world SW conditionsPower Management complexity is growing

ASIC Power Management Features Verified

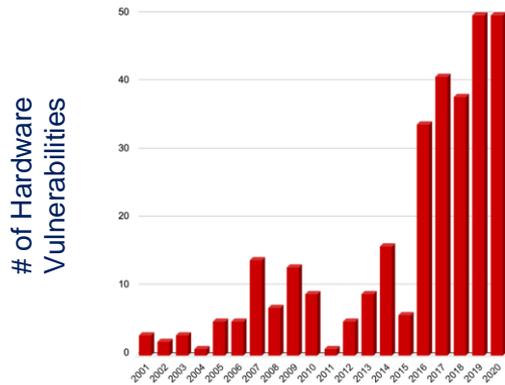


Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study  
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- Power Verification is increasingly complex
- Power Analysis Methodologies increasingly sophisticated
- IC Design Power Issues are in fact “Power Bugs”

# Security Bugs



Source: NIST/MITRE 12/2020



Valytic Consulting

- Security Bugs can be catastrophic!
  - Increase in number of hardware vulnerabilities in recent years
  - New breeds of bugs – security vulnerabilities that can be harder to detect.
  - CIA bugs: Confidentiality, Integrity, Availability
  - Complex attack scenarios such as Cache Timing Side Channel Attack
  - Security verification e.g. requirements driven threat modeling
    - Build a Threat DB – leverage CWE DB

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# FuSa Bugs



Projects Working on Safety Critical Design



Percentage of ASIC/IC projects working on a safety critical development standard (e.g. DFC-254, ISO26262, IEC60601, IEC61508, etc.)

Source: Wilson-Research Group and Mentor. © Siemens Business, 2020 Functional Verification Study.  
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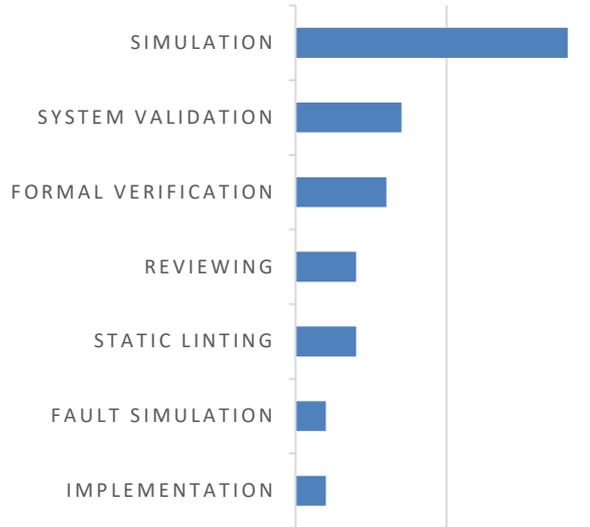
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- Guess what? FuSa Bugs can be catastrophic!
  - Normal operation works fine – but ASIL targets can be missed
  - Systematic Failures in the Design Affecting Functional Safety Requirements
  - Complexity: New Bugs injected into Non-Trivial Functional Safety Mechanisms
  - Fault-injection/fault-simulation and FMEA/FMEDA is necessary to find these Bugs

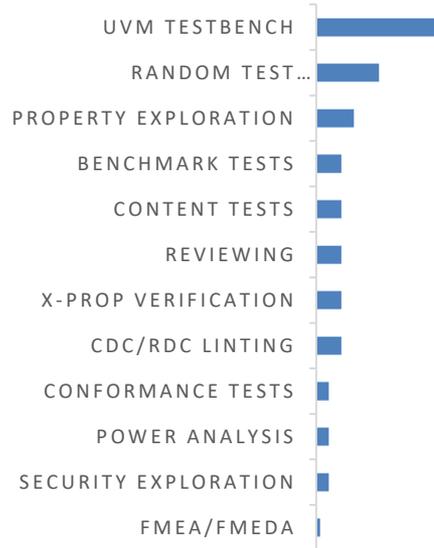
# How are bugs found?

**(FAKE DATA)**

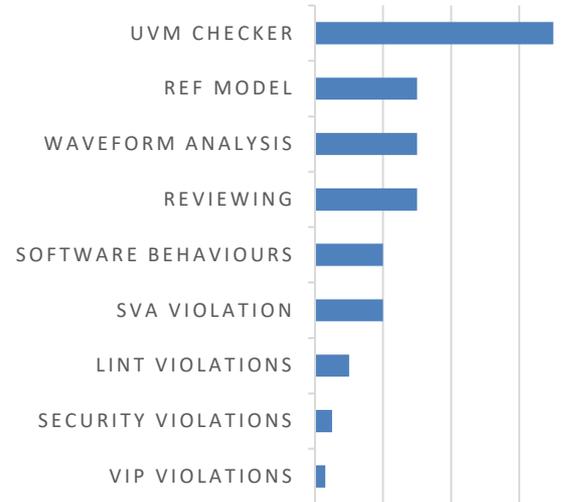
## METHODOLOGY



## STIMULUS



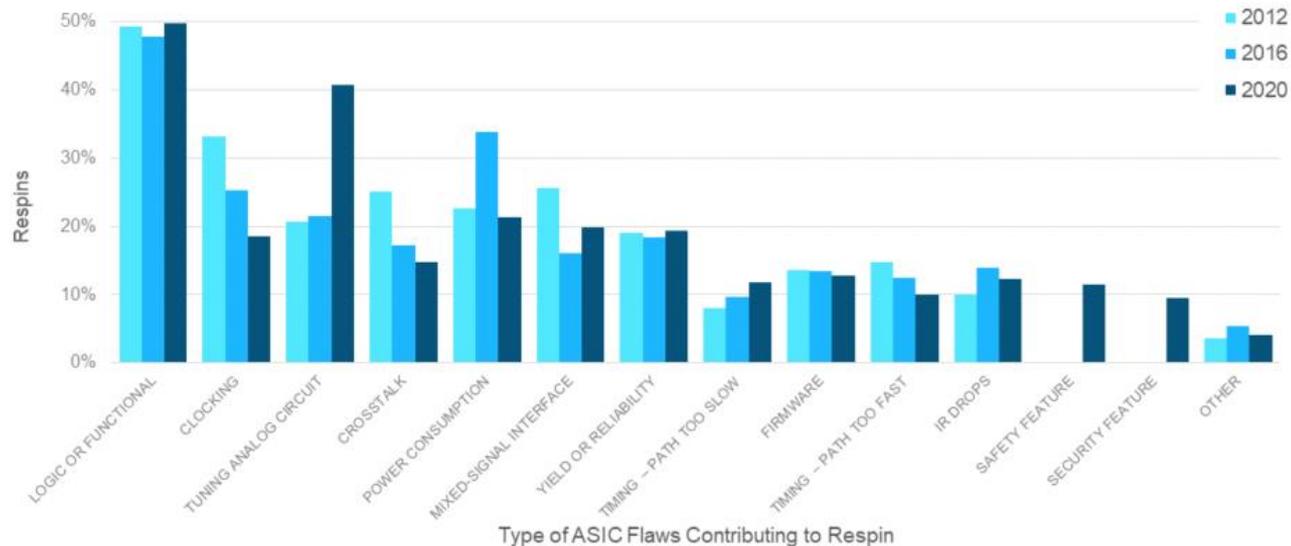
## CHECKER



*How effective is your verification? Where to invest? Where to divest?*

# What are the Root Causes of Bugs?

## ASIC Type of Flaws Contributing to Respin



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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Figure 12-3. Types of Flaws Resulting in Respins

- <https://blogs.sw.siemens.com/verificationhorizons/2020/10/27/prologue-the-2020-wilson-research-group-functional-verification-study/>

# Continuous Improvement through RCA

## Design Root Causes

- Why was the bug introduced into the RTL codebase?
  - Poor coding styles?
  - Complexity?
  - Code Churn?
  - Specification Error?
  - Schedule constraints?
  - Etc...

## Verification Root Causes

- Why was the bug missed by previous verification?
  - Stimulus gap?
  - Checking gap?
  - Coverage hole?
  - Testplan gap?
  - Methodology gap?
  - Specification Error?
  - Poor coding style?
  - Resource constraints?
  - Schedule constraints?

# THE COST OF BUGS

What is the Cost of Finding Bugs?  
What is the Cost of NOT Finding Bugs?

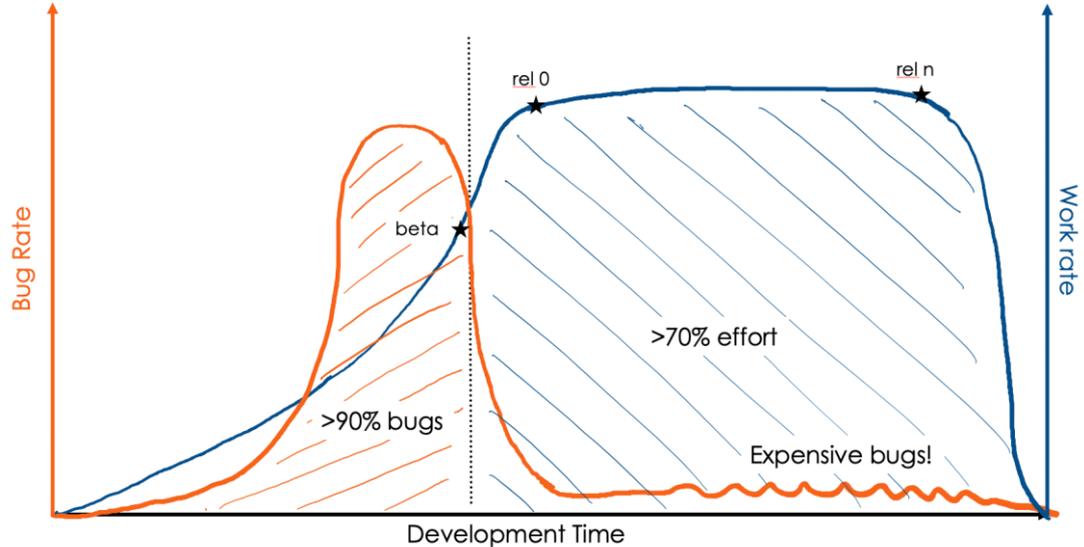
# The Cost of Finding Bugs

## When are Bugs Found?...The Sooner the Cheaper!!

**OPINION:** most bugs should be flushed out in the early stages (say with 30% of the work) these are the easy finds

Verification work (consumption of resources and human effort to find, debug and fix) is disproportionately high for the remaining 10% of bugs

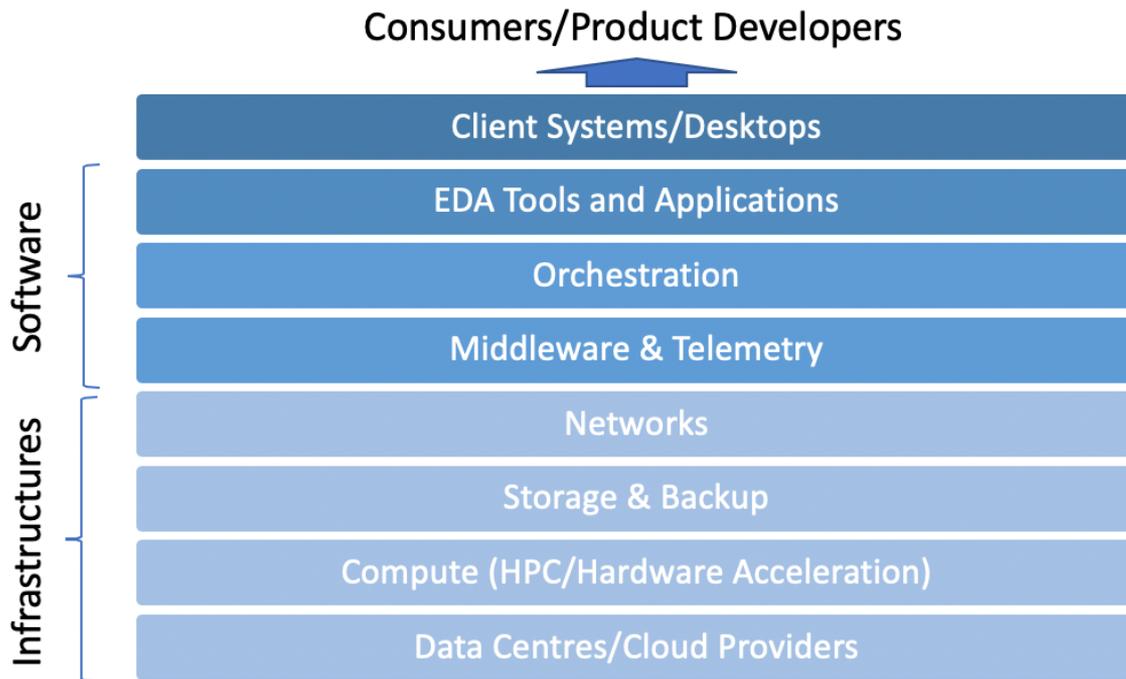
Focus workflow and methodology improvements on this later stage for the biggest ROI



*The last 10% are often the critical ones!*



# The Cost of Finding Bugs: The Engineering Platform



# Understanding your verification ROI



# Fixed capacity, fixed architecture problem

## Scenario

Resource scarcity  
Inflexible architecture  
Incomplete data to forecast  
need

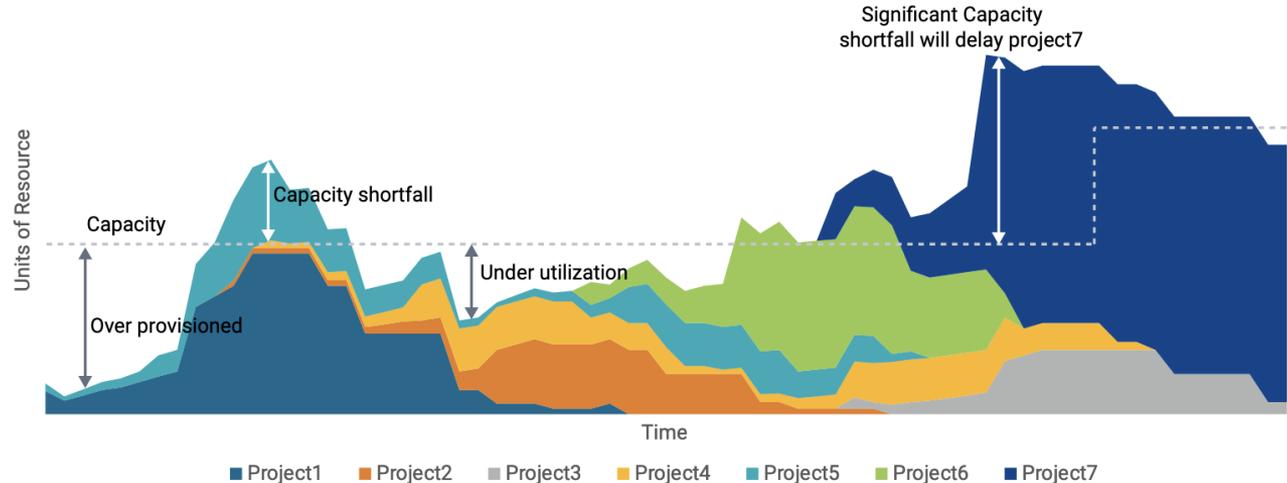
## Leading to...

Project delays  
Waivers and risk

## Drives

Extra spend on compute  
Exploration for alternatives

On-Prem Resource Demand Forecast



[Source](#) – Made in the cloud – Understanding the case for IC hardware development in the cloud. Bryan Dickman, Valytic Consulting, Joe Convey Acuerdo Ltd., Teng Kiat-Lee Synopsys, Inc., Sandeep Mehndiratta Synopsys, Inc.

# CLOUD MATTERS!

Run faster, run leaner,  
innovate sooner, save money,  
understand your engineering  
platform costs better *and* get  
best-in-class Business  
Continuity thrown in for  
free...

## Why isn't everyone doing it?

Levelling-up for smaller organizations to compete  
against larger ones

For larger operations cloud brings capacity flexibility  
when there are workload peaks and troughs

An opportunity to do things differently

## But....

- When is the right time to shift?
- What about lifting and shifting workflows?
- Contractual models for adoption...?

**Good data and analytics matters more!**

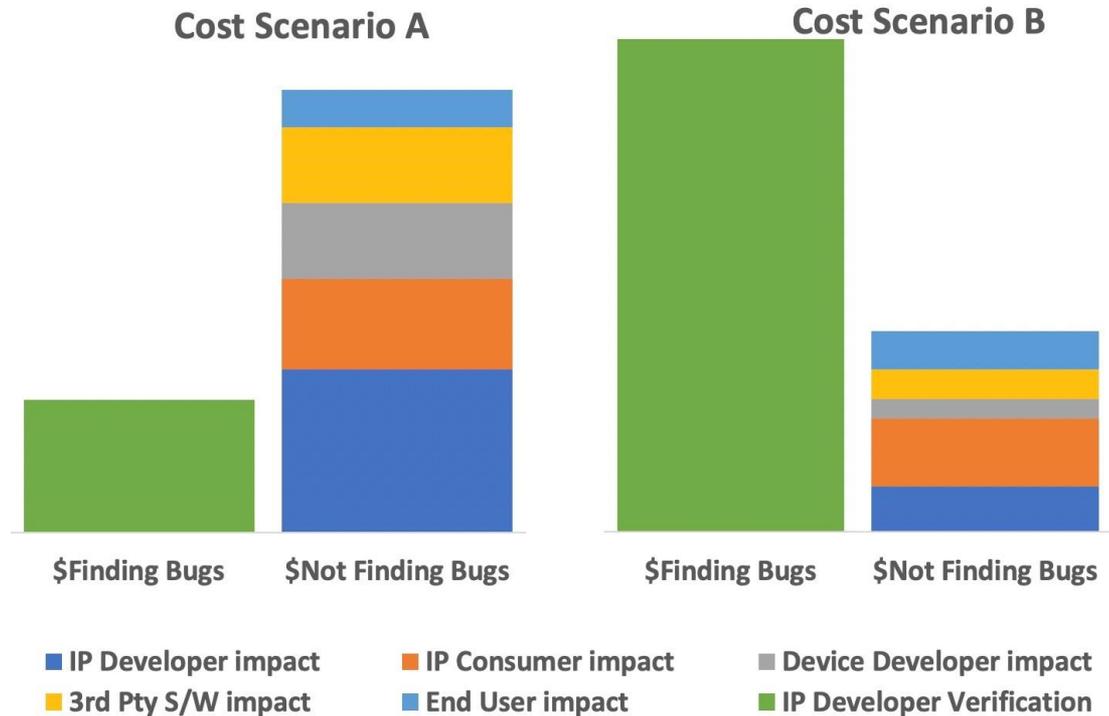
# Do you have enough data to reason about your risk profile?

## Are you scenario A...?

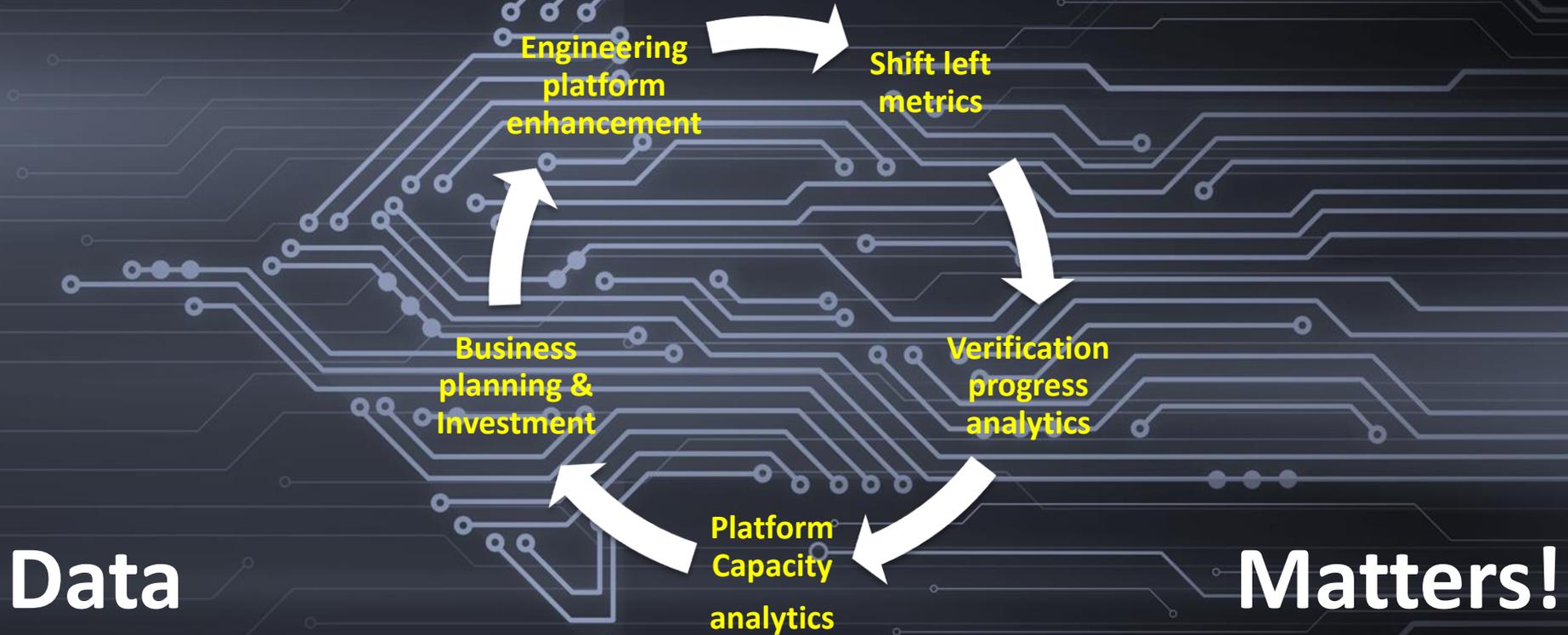
cost-to-find low, but high risk/impact regretting not having spent enough on verification

## Or, are you scenario B...?

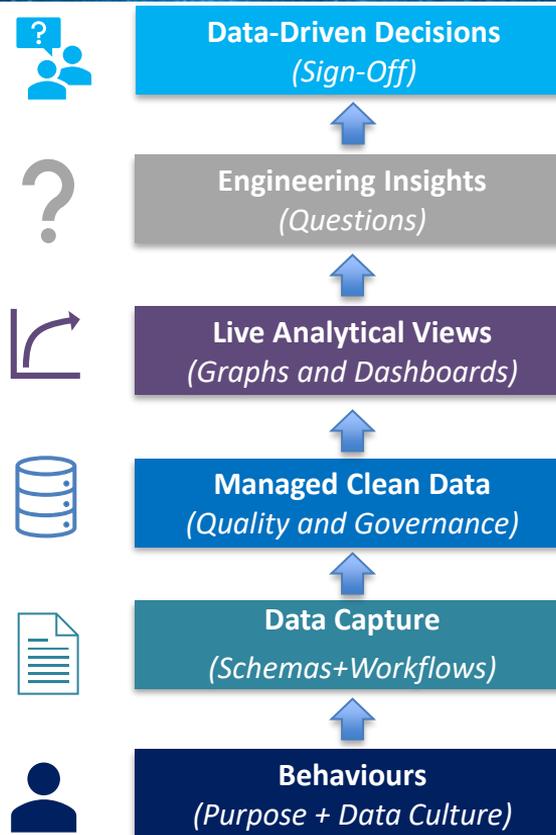
cost-to-find high with impact risk/cost low wondering if you are spending too much?



# Invest in data to make better decisions, sooner



# Data-Driven decision making reduces Bugs



So, the Point is....

**BANGS!**



# The Quest for Bugs

<https://www.acuerdo.co.uk/thequestforbugs>



**The Quest for Bugs:  
“Dilemmas of  
Hardware Verification”**

(Navigating the Challenges)

*12 minute read*

Bryan Dickman, Valytic Consulting Ltd.,  
Joe Convey, Acuerdo Ltd.



**The Quest for Bugs:  
“The Bugs of Power”**

(Understanding Power Bugs and how  
to find them in large ASICs by using  
Emulator Power Analysis)

*10 minute read*

Bryan Dickman, Valytic Consulting Ltd.,  
Joe Convey, Acuerdo Ltd.



**The Quest for Bugs:  
“Deep Cycles”**

(Approximating Silicon with FPGA Prototyping)

*10 minute read*

Bryan Dickman, Valytic Consulting Ltd.,  
Joe Convey, Acuerdo Ltd.



**The Quest for Bugs:  
“Correct by Design!”**

(Understanding Architecture Design Bugs  
and how to avoid them in large ASICs by  
using Virtual Prototyping)

*10 minute read*

Bryan Dickman, Valytic Consulting Ltd.,  
Joe Convey, Acuerdo Ltd.

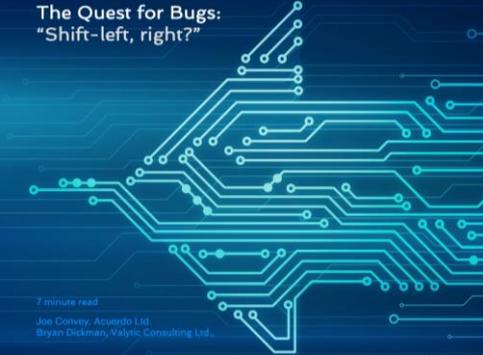


**The Quest for Bugs:  
“Security Matters!”**

(Avoiding security bug strikes with hardware security  
verification)

*10 minute read*

Bryan Dickman, Valytic Consulting Ltd.,  
Joe Convey, Acuerdo Ltd.



**The Quest for Bugs:  
“Shift-left, right?”**

*7 minute read*

Joe Convey, Acuerdo Ltd.  
Bryan Dickman, Valytic Consulting Ltd.

THANK-YOU

