Accelerating Verification and Implementation

With Machine Learning for Electronic Design Automation

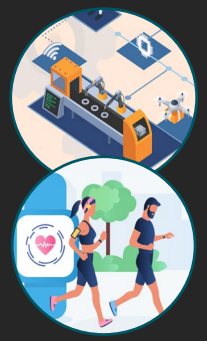
Frank Schirrmeister, Sr. Group Director, Solutions & Ecosystem

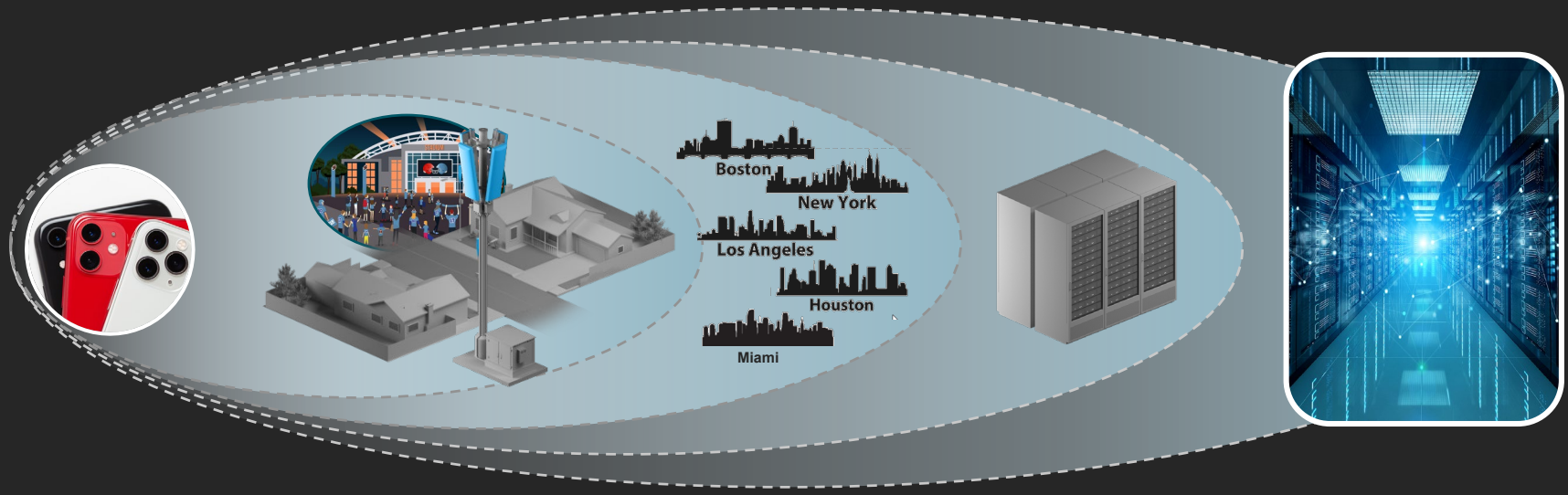
DVCLUB, November 23rd 2021

cadence®

Intelligent Systems: Ubiquitous Hyperconnectivity

Consumer | Hyperscale | Mobile | Communications | Automotive | Aero / Defense | Industrial | Healthcare





Sensor Edge | **Device Edge** | **Far Edge** | **Middle Edge** | **Near Edge** | **Cloud Data Center**

Data ← → Data

000111 1010 11 111100000011 000111 1010 011111001000 11 111100000011 000111 1010 011111001000 000111 1010
1110001010 1010000011110000 1110001010 1110001010 1010000011110000 1110001010 **1110001010** 1110001010

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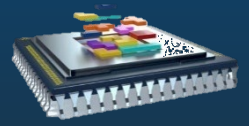
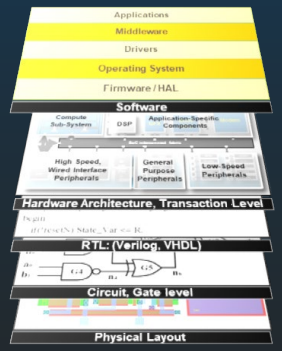
EDA **Enables** AI/ML Designs

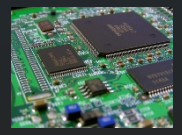


IP and Subsystems

Verification



Implementation



Board and Package

Systems

IP Selection

"Reuse the right building blocks"

DSPs, Interfaces, Analog

HW/SW Verification

"Is it functionally correct?"

Hardware/Software, Power, Architecture, Safety, Security

Chip Implementation

"Optimized, advanced-node implementation"

Performance, Power, Cost

Packaging PCB Integration

"Silicon into packages and parts into PCBs and 3D-IC heterogeneous integration"

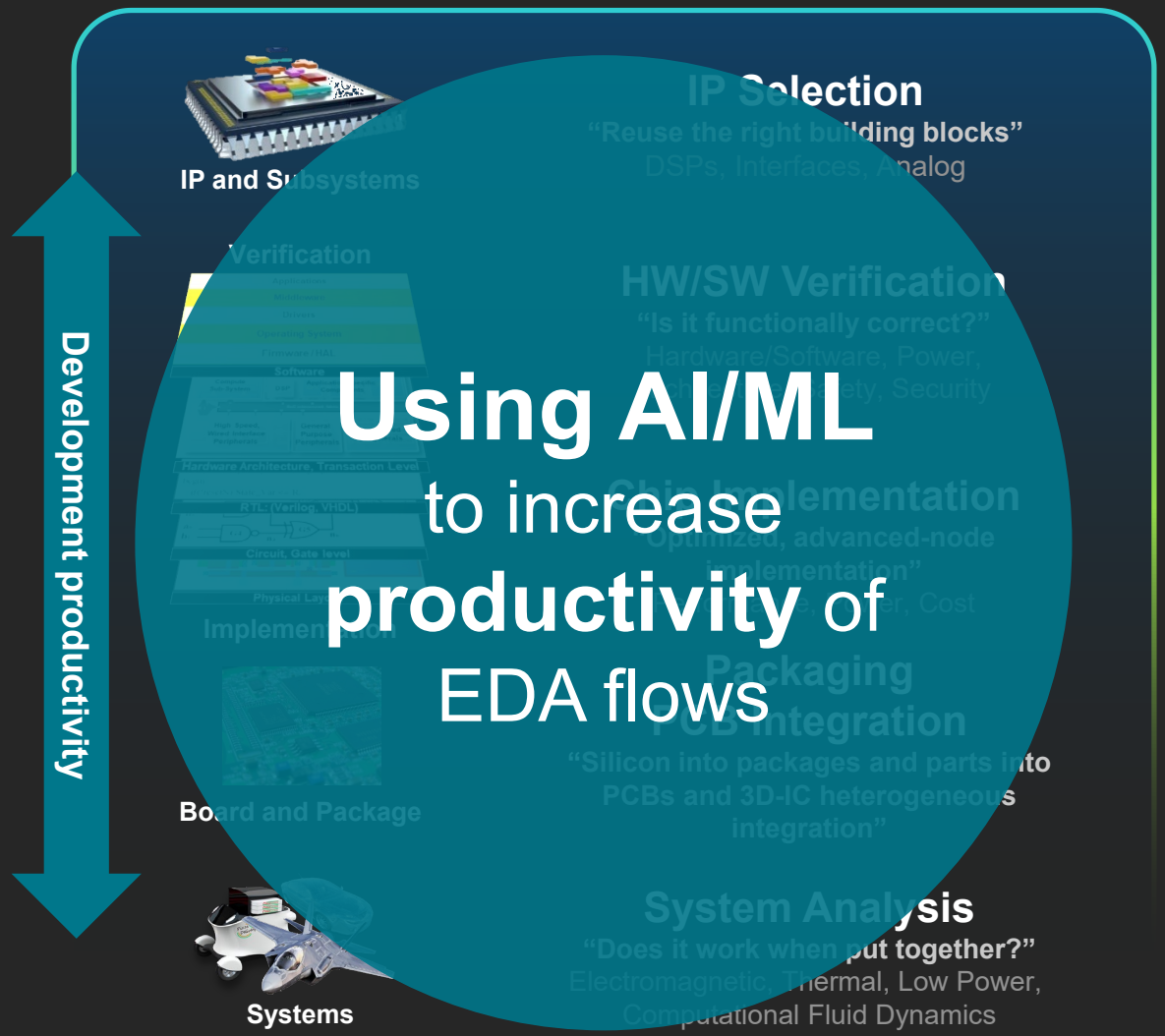
System Analysis

"Does it work when put together?"

Electromagnetic, Thermal, Low Power, Computational Fluid Dynamics

Optimized flows to **enable AI/ML** chips and systems (for users)

AI/ML is **Enabling EDA** too!



Optimized **flows** to **enable AI/ML** chips and systems

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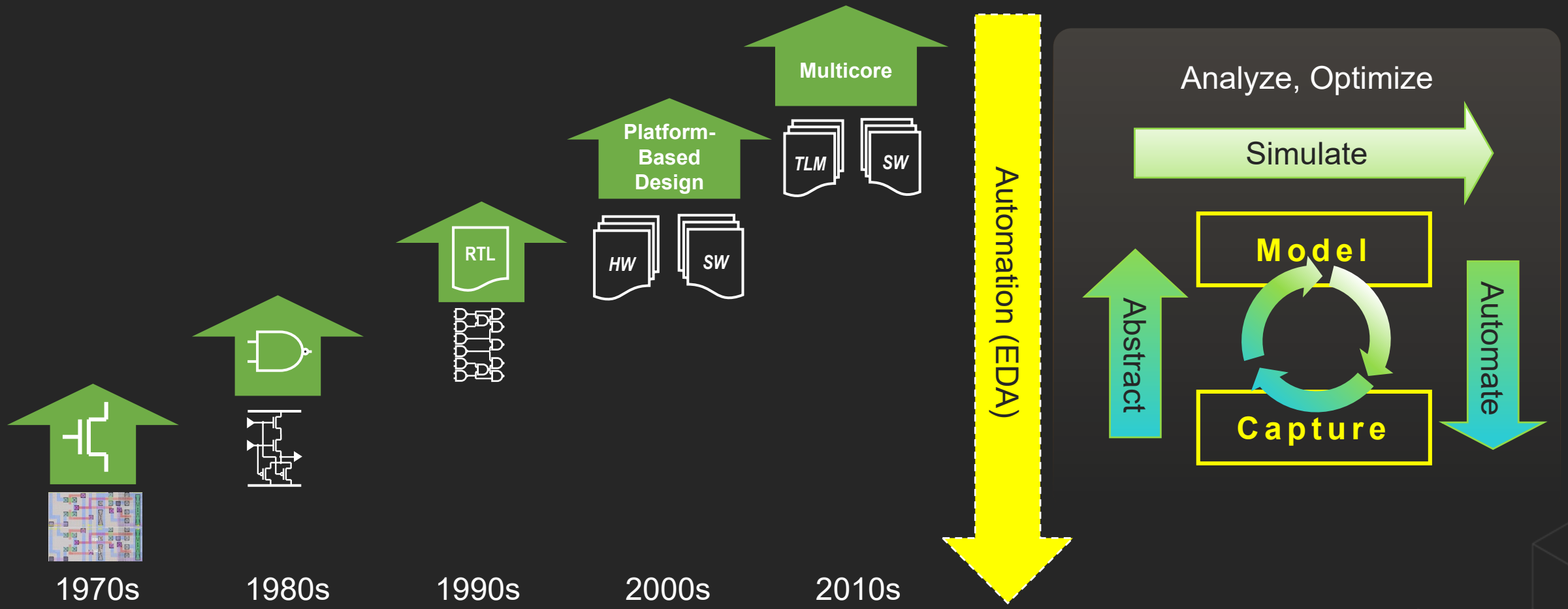
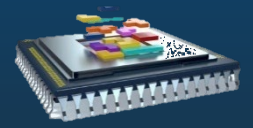
EDA Keeps Design Cost in Check – Commonalities



Targeting “High Effort” Aspects of the Design Flows



IP and Subsystems

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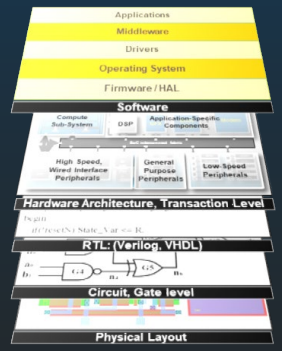

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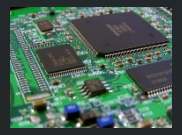
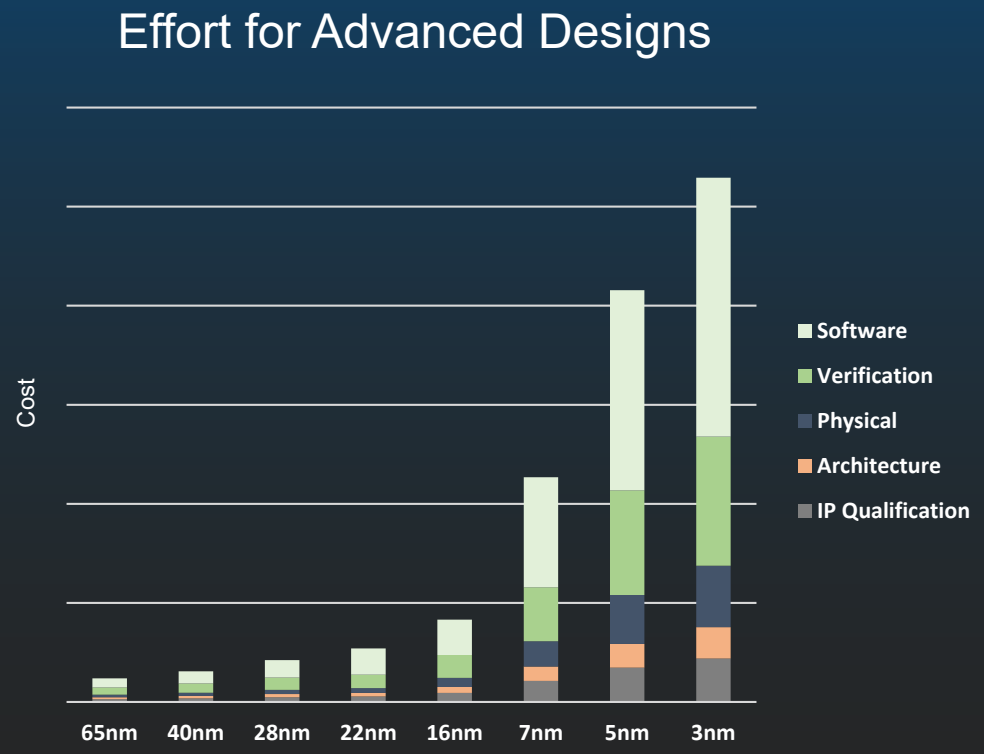
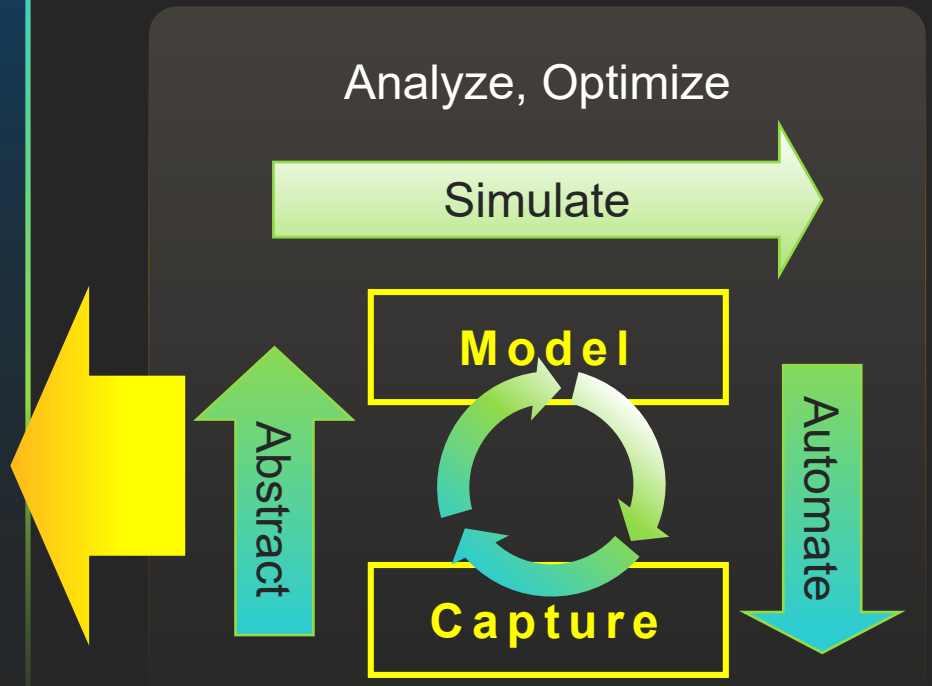


Board and Package

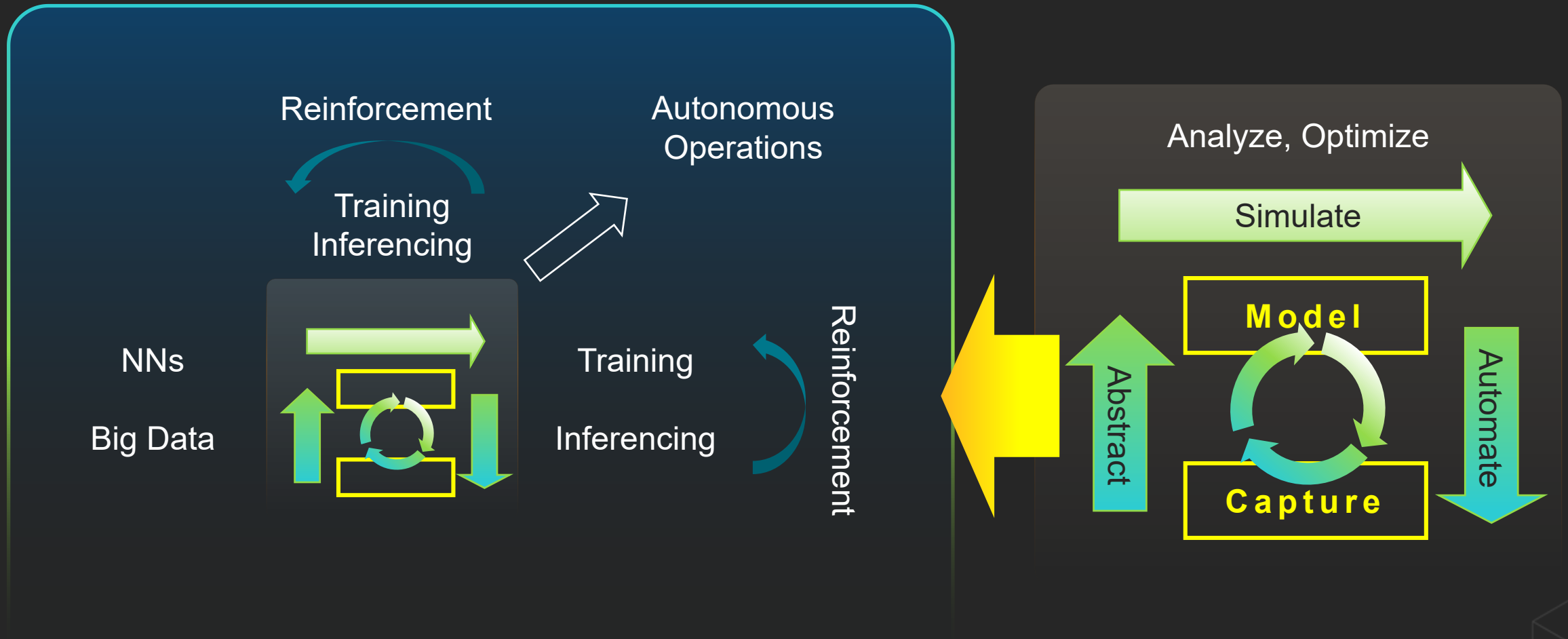
Systems



Source Data: IBS 2021, Cadence

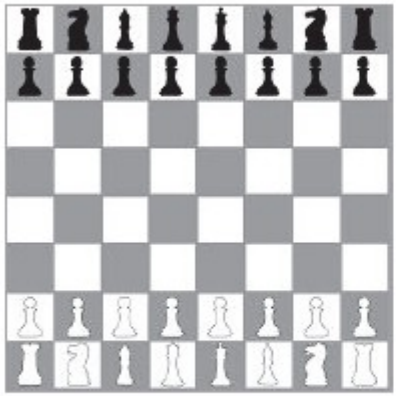


EDA and AI/ML



So You Think Chess & Go Were Complex?

Chess

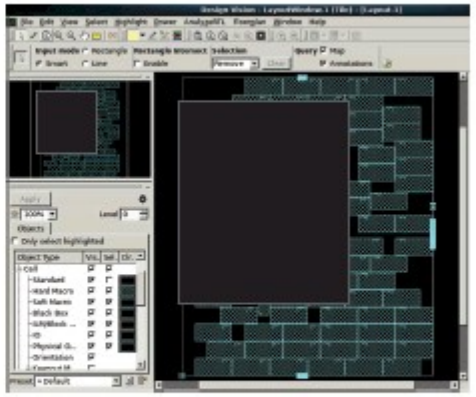


Number of states ~ 10^{123}

Go

Number of states ~ 10^{360}

Chip Placement



Number of states ~ 10^{9000}

Architecture

Power

Performance

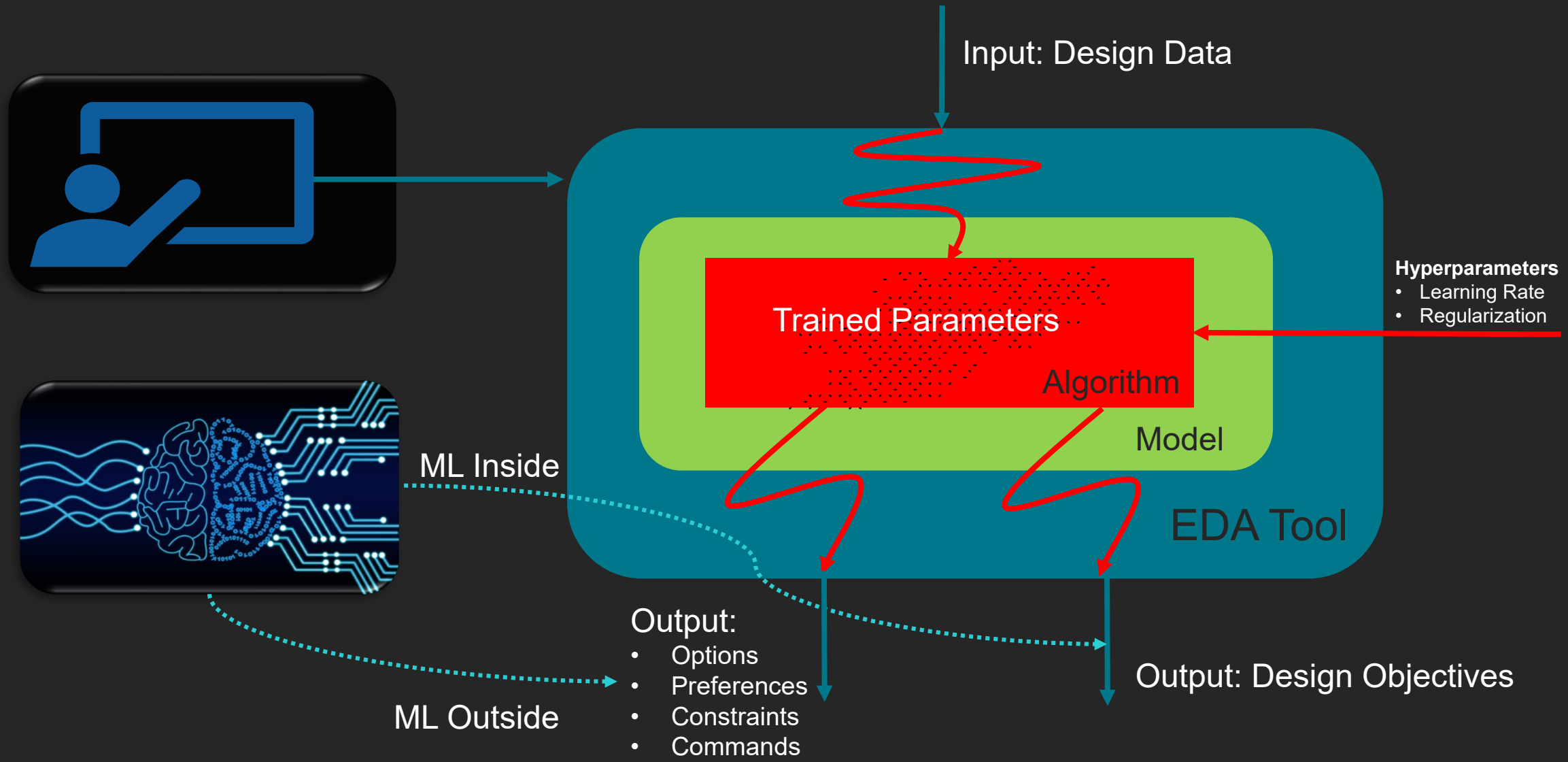
Cost

Software

“More than Moore”

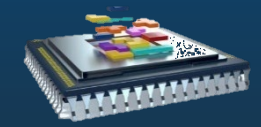
Source: The Next Platform, “Google Teaches AI to Play the Game of Chip Design”, https://bit.ly/3Bwxg8p, Cadence

ML in Electronic Design Automation



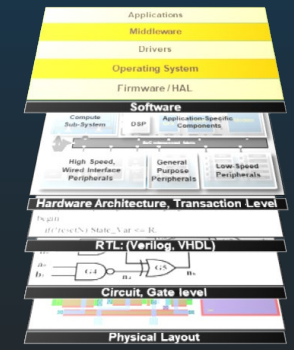
AI/ML Opportunities in EDA

Functional Verification	• **Simulation** smarter and faster regressions • **Formal verification** formal proof orchestration
Digital Implementation	• **Digital implementation "ML inside"** delay prediction • **Digital implementation "ML outside" f**low optimization
Library Characterization	• **Library c**haracterization with ML-based prediction
Custom IC Implementation	• **SPICE simulation** ML for accurate response surface models • **Custom implementation**: Layout and analog placement
Design for Manufacturing	• **ML-DFM**: Predicting unknown yield limiting hotspots
PCB Synthesis	• **PCB design** placement, via, routing, power delivery, analysis
System Design and Analysis	• **System analysis "Smart Sweep"** Predict eye openings

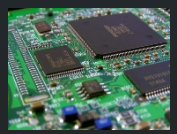


IP and Subsystems

Verification



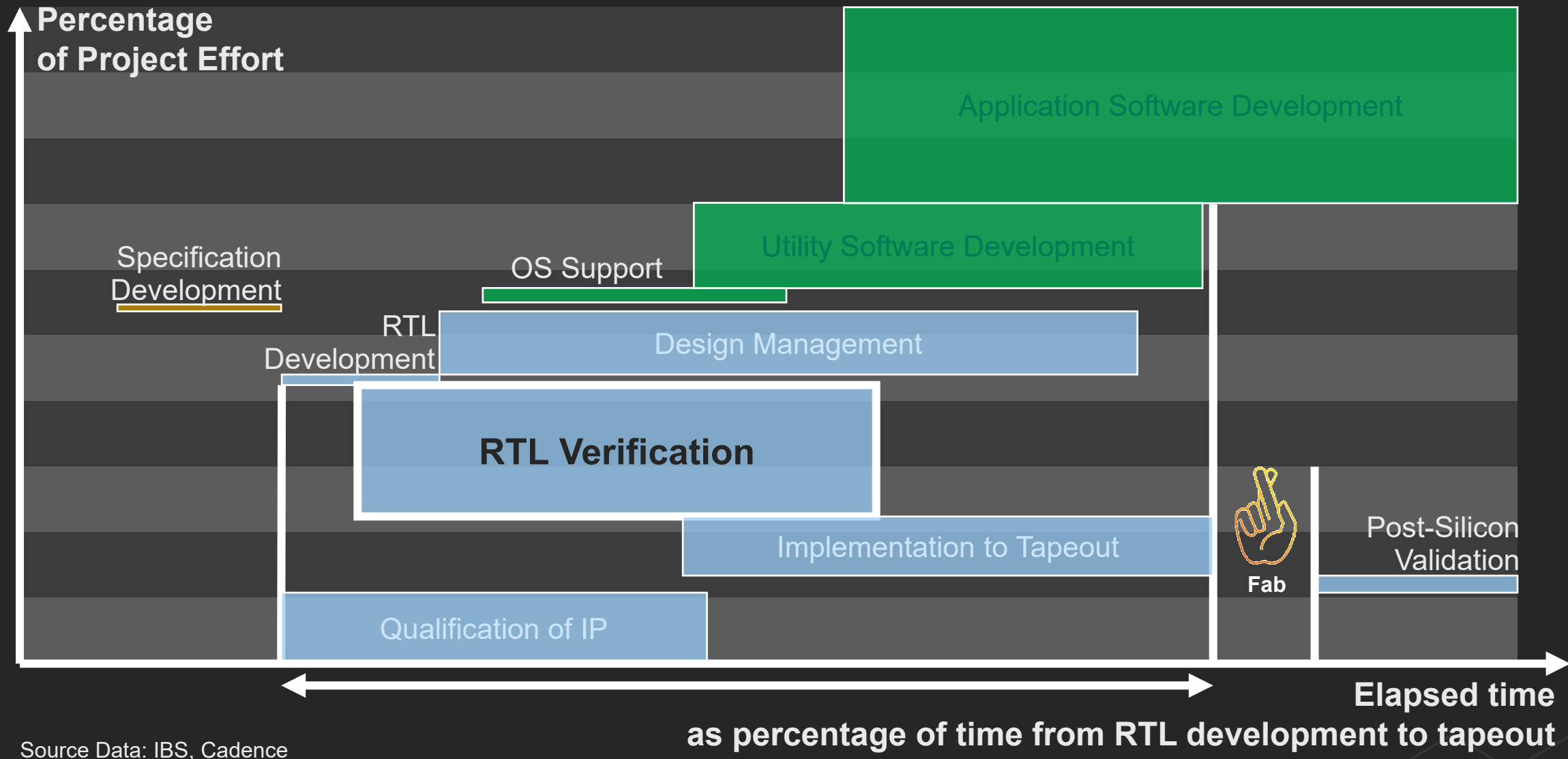
Implementation



Board and Package

Systems

Verification as Part of Chip Development Efforts



Source Data: IBS, Cadence

ML in Functional Verification

Baseline

CPU$_1$ T1.1 T1.2 T1.3 T1.4 ...

CPU$_2$ T2.1 T2.2 ...

CPU$_m$ Tm.1 ...

Regression finished

Time

Machine Learning

CPU$_1$ T1.1 T1.3 T1.9 ...

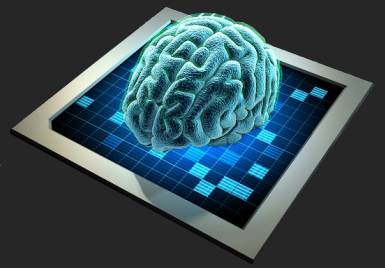
CPU$_2$ T2.1 T2.2 ...

CPU$_m$ Tm.1 ...

CPU$_0$ Machine Learning

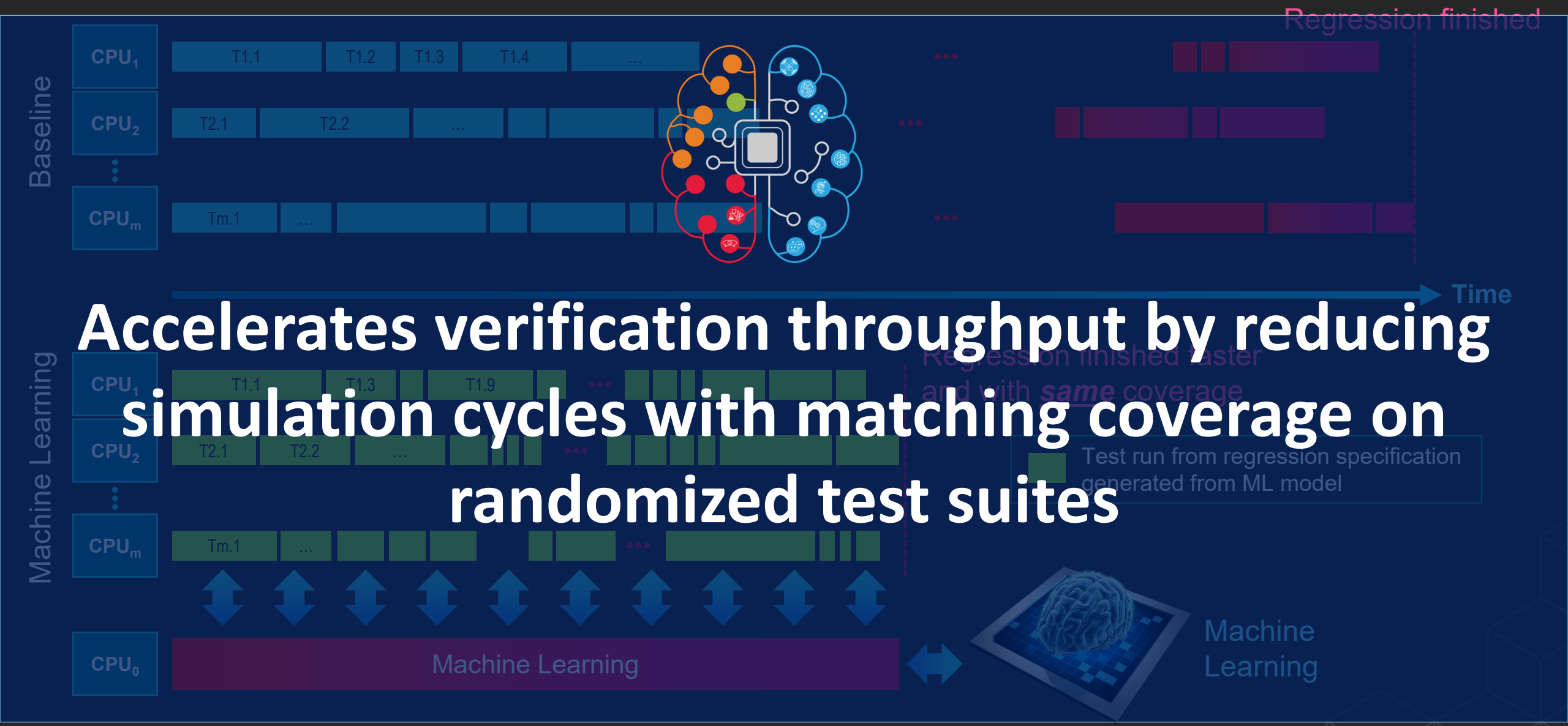
Regression finished faster and with ***same*** coverage

Test run from regression specification generated from ML model



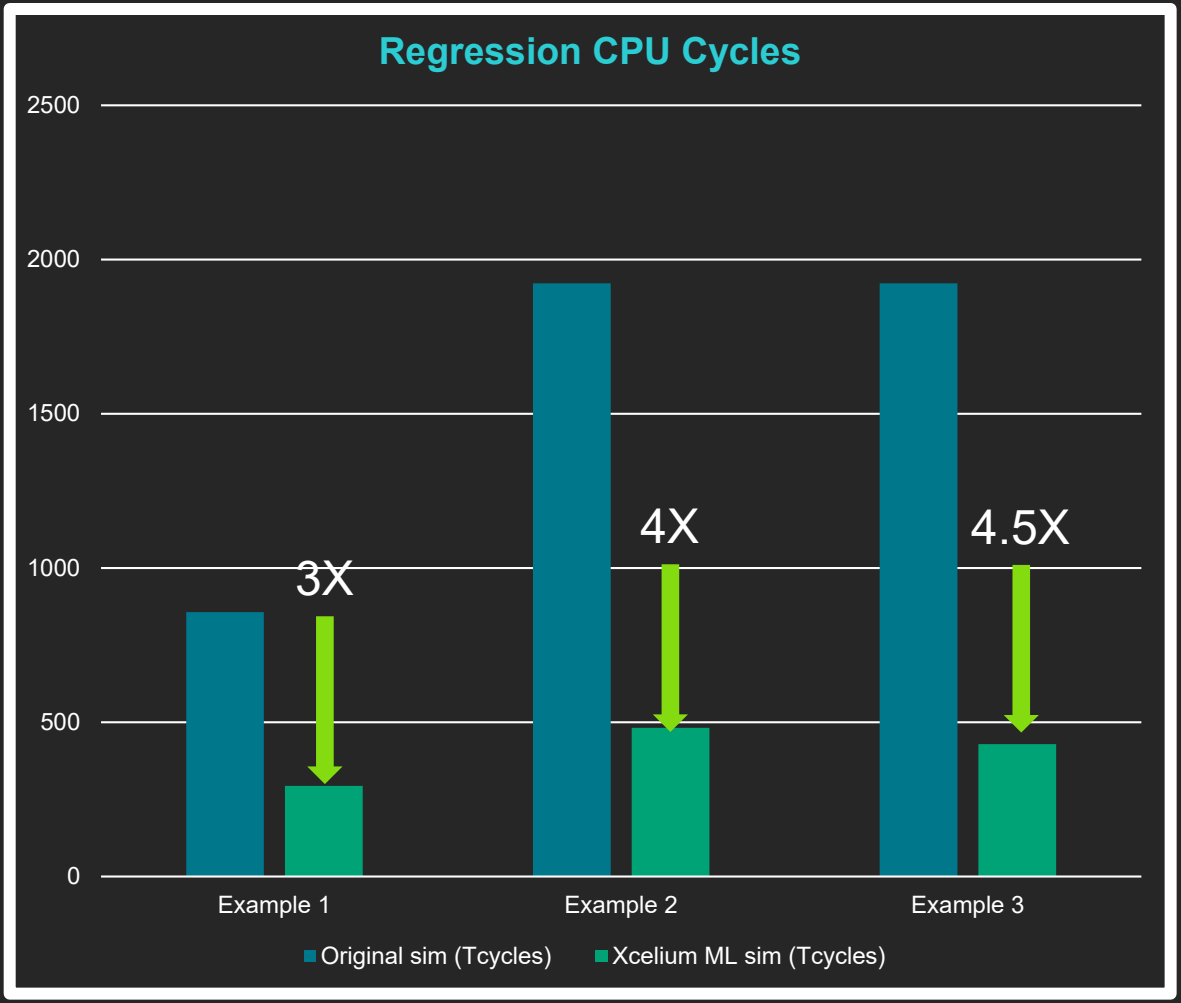
Machine Learning

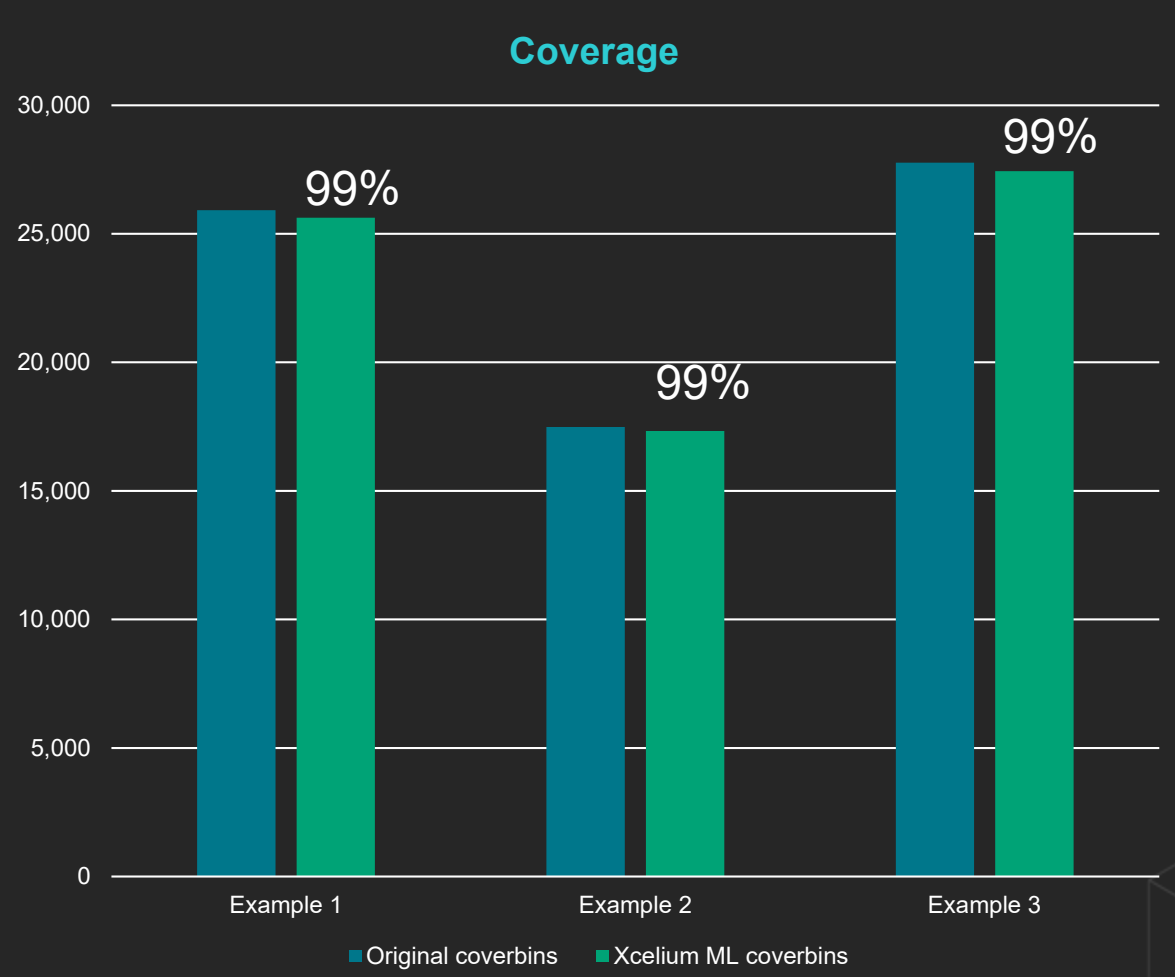
ML in Functional Verification



Accelerates verification throughput by reducing simulation cycles with matching coverage on randomized test suites

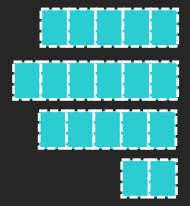
Xcelium-ML Up to 5x efficiency at same coverage





Xcelium ML for Verification Throughput

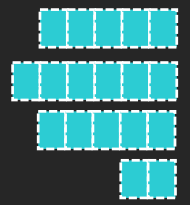
Randomized Test Suite **Run N**



Up to 5X faster
Same coverage

Machine Learning

Randomized Test Suite **Run N+1**



"Kioxia has effectively utilized Xcelium simulation for a variety of our designs, and it addresses our ever-growing verification needs. With the new Xcelium ML, we've seen a **4X shorter turnaround time** in our fully random regression runs **to reach 99% function coverage of original**, and plan to use this technology in production designs to shorten the time to market for Kioxia's business."

Kazunari Horikawa
Senior Manager, Design Technology Innovation Division
Kioxia Corporation

KIOXIA

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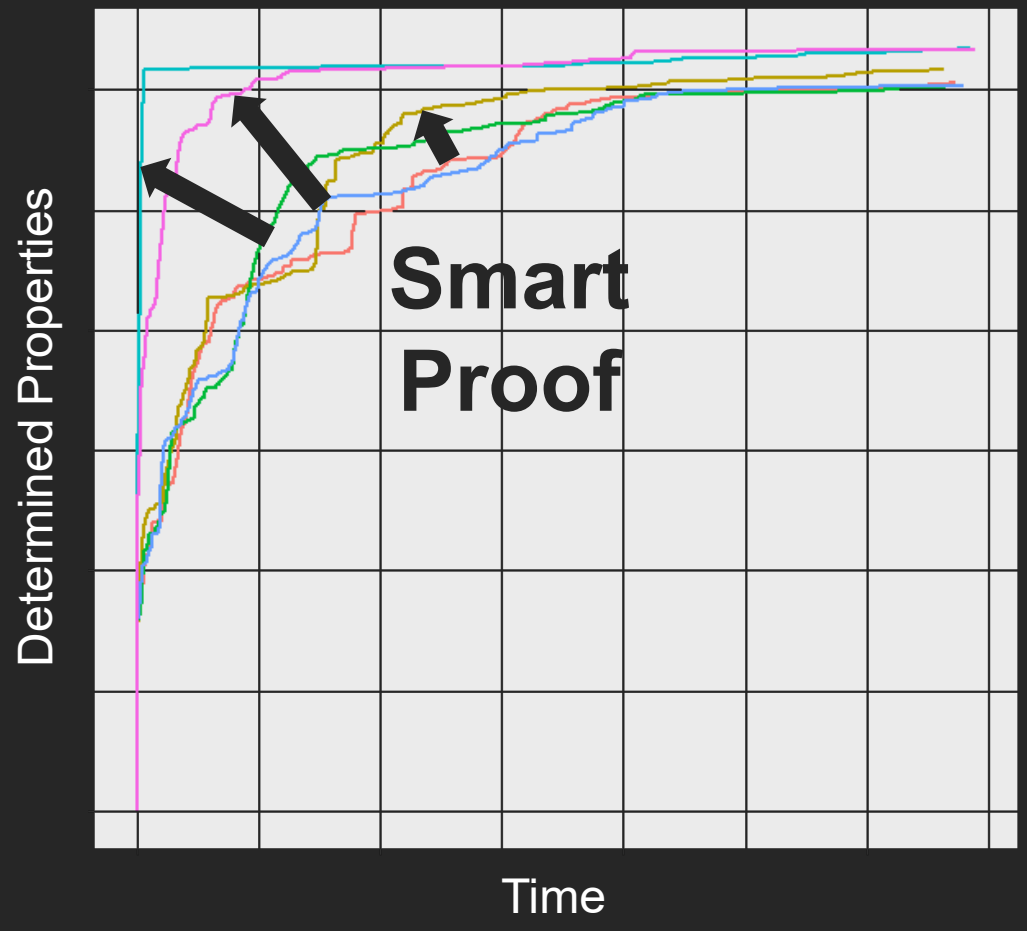
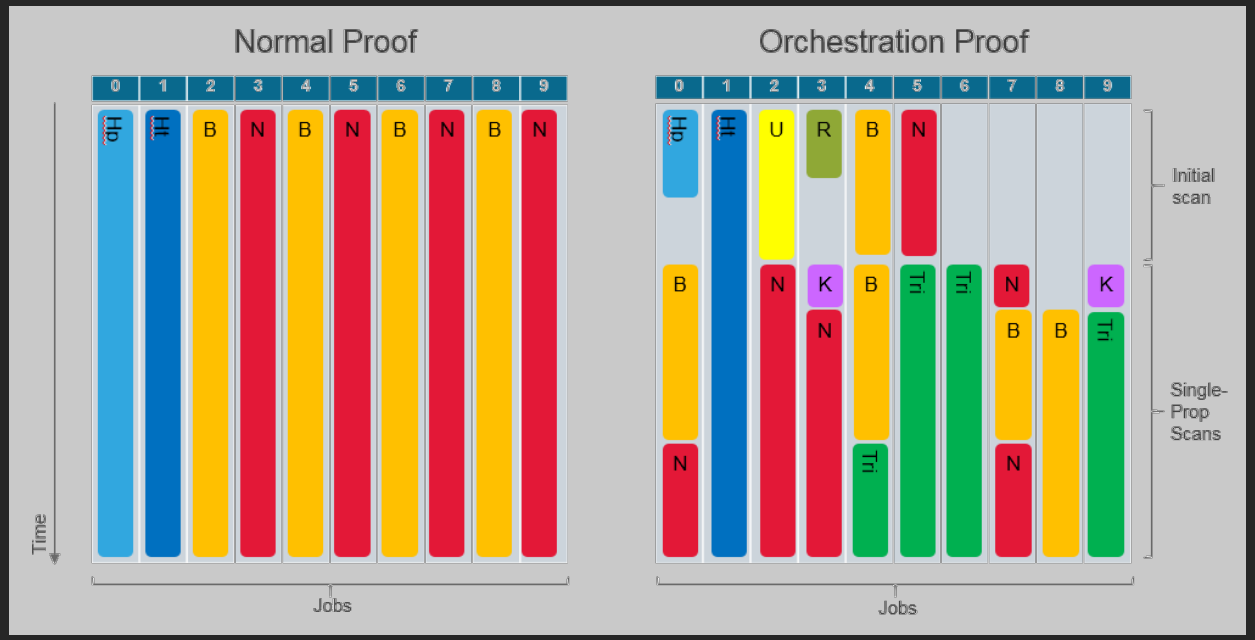
Smart Proof in Formal Verification

Optimize Resources, Reproduce Previous Runs





Reinforcement learning dynamically adjusts engine selection, time limits, parallel threads, etc.

Smart Proof in Formal Verification

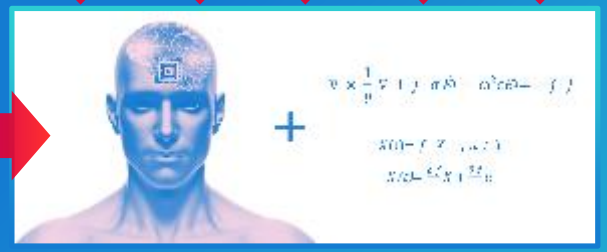
Computational logistics technology for formal throughput

Inside Cadence® R&D

Proof Algorithm 1 … Proof Algorithm N

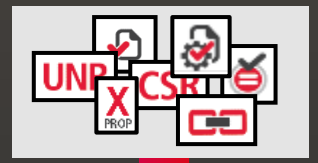
Parameter 1 … Parameter N Parameter 1 … Parameter N

Training set of proof problems



Knowledge Graph and Machine Learning

Released Product



Proof Apps

Design

Testcase	Baseline	Smart Proof	Gain
A	50%	59%	1.2X
B	69%	69%	1.0X
C	12%	25%	2.1X
D	44%	83%	1.9X
E	57%	94%	1.6X
F	68%	69%	1.0X
Total	53%	71%	1.3X

* Average results from typical regressions; actual results may vary

Smart Proof in Formal Verification

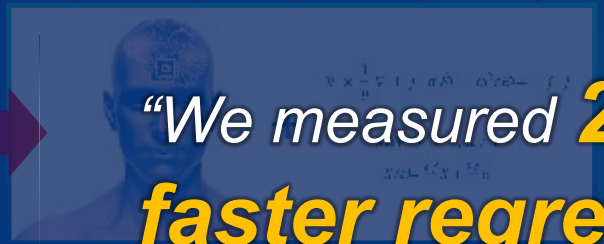
Computational logistics technology for formal throughput

Third-Generation JasperGold® Formal Verification Platform

Inside Cadence® R&D

Proof Algorithms

Training set of proof problems



Knowledge Graph and Machine Learning

Smart Proof Solver

Released Product

Proof Apps

Smart Proof Solver

*"We measured **2X faster** proofs out of the box, **5X faster regressions,** and non-converged properties **reduced by 50%**"*

-Mirella Negro Marcigaglia, digital design verification manager, STMicroelectronics

			Gain
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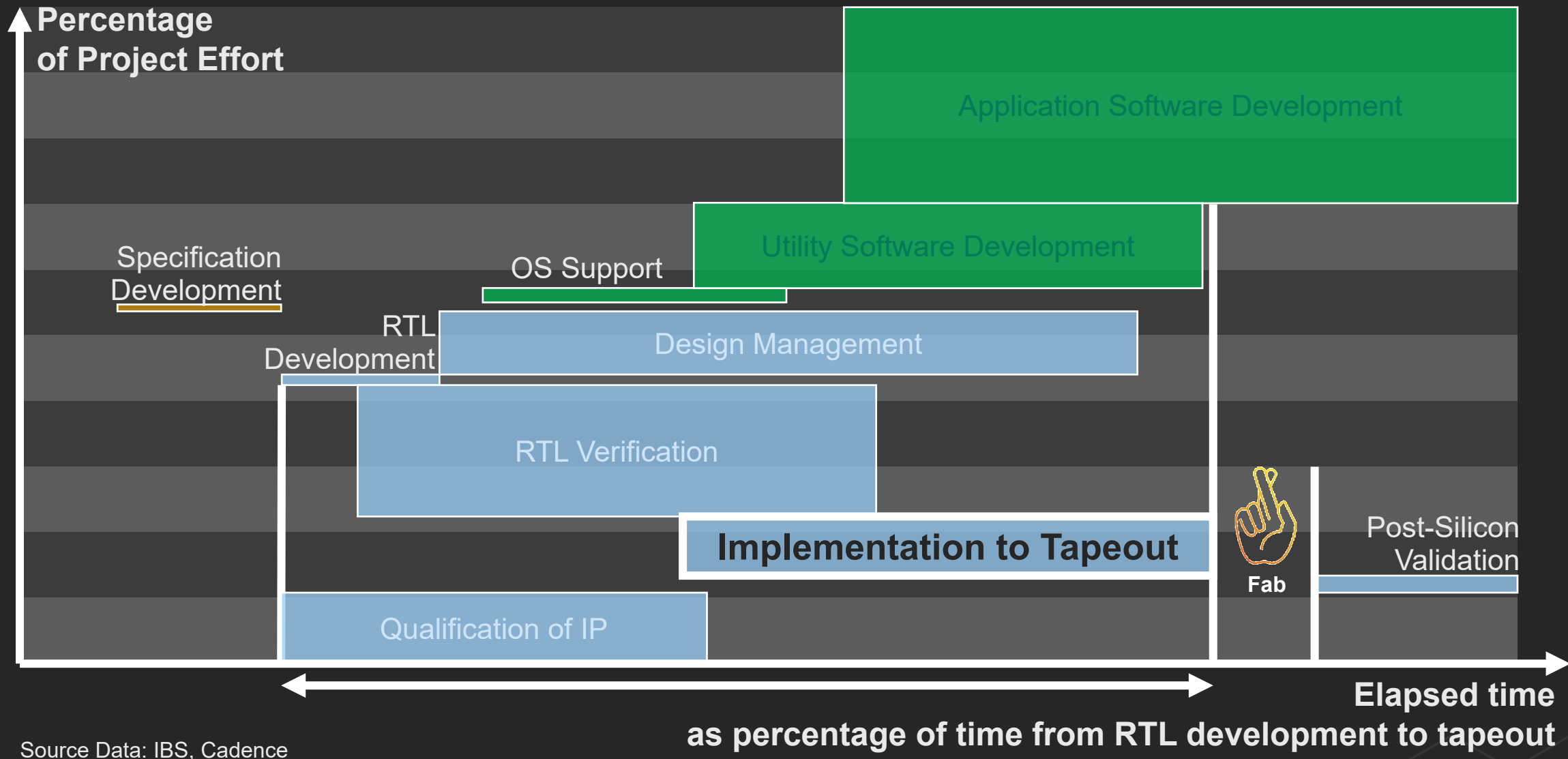
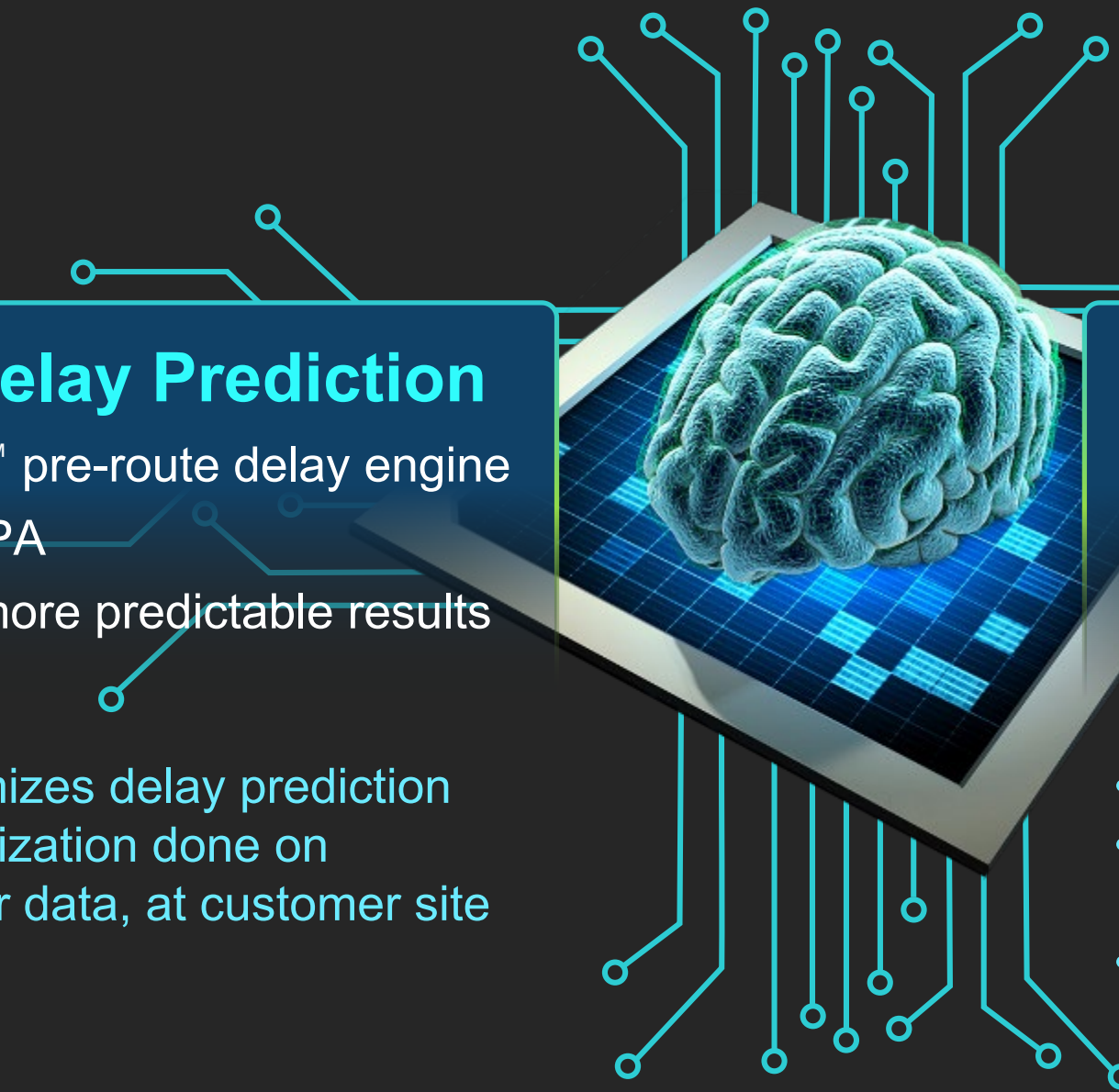
Implementation as Part of Chip Development Efforts



Source Data: IBS, Cadence

ML for Better Performance and Productivity



ML Delay Prediction

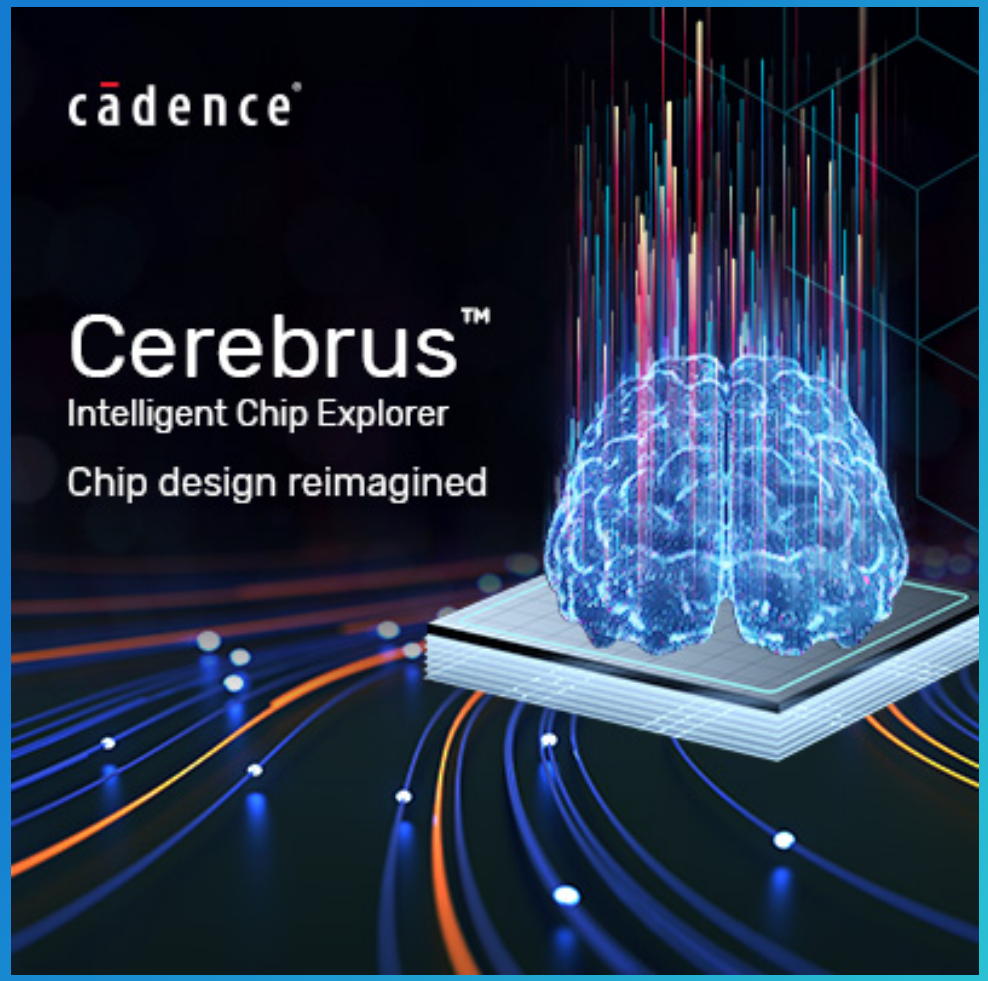
- Innovus™ pre-route delay engine
- Better PPA
- Faster, more predictable results

- ML optimizes delay prediction
- All optimization done on customer data, at customer site

Intelligent Chip Explorer

- Automated smart design flows
- Productivity improvements

- ML optimizes flow (SI congestions)
- Adjusting tool and library options, constraints, parallel runs in cloud
- All optimization done on customer data, at customer site



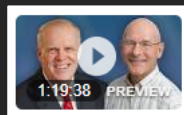
RENESAS

To efficiently maximize the performance of new products that use emerging process nodes, digital implementation flows used by our engineering team need to be continuously updated. **Automated design flow optimization is critical for realizing product development at a much higher throughput.** Cerebrus, with its innovative ML capabilities, and the Cadence RTL-to-signoff tools have provided automated flow optimization and floorplan exploration, improving design performance by more than 10%. Following this success, the new approach will be adopted in the development of our latest design projects.

Satoshi Shibatani, director, Digital Design Technology Department, Shared R&D EDA Division, Renesas

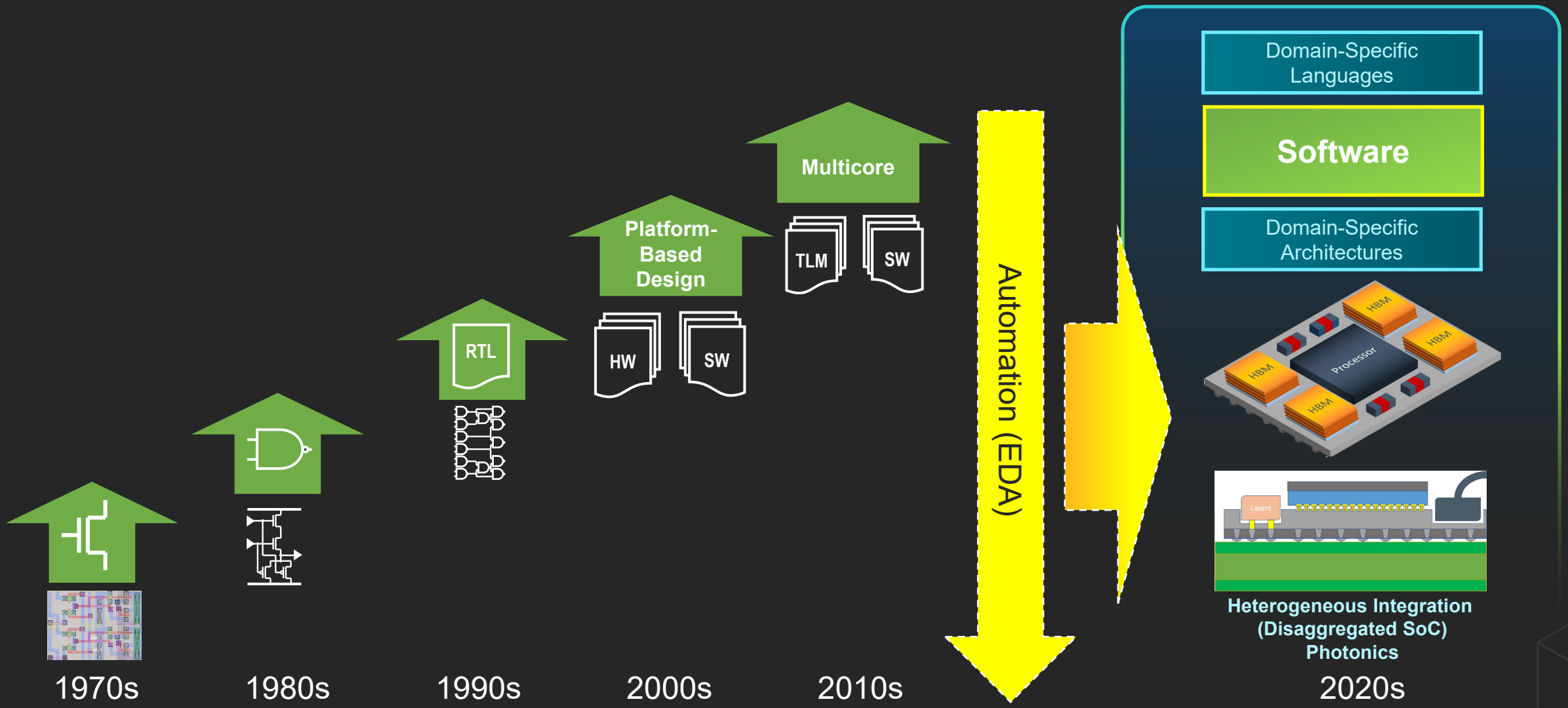
Summary

Next: “More than Moore”



John Hennessy and David Patterson 2017 ACM A.M. Turing ...

YouTube · Association for Computing Machinery (ACM)
Jun 4, 2018



AI/ML Productivity Improvements - Some Examples

Functional Verification	Up to **5X reduction in simulation cycles (**same coverage) Up to **4X** (2X avg.) **better out-of-the-box proofs**
Digital Implementation	Up **20% better PPA**, up to **10X productivity**
Library Characterization	**Accelerated library development** Example: 47% of libs interpolated 98%+ pass rate
Custom IC Implementation	Accurate **response surface model** of the device or block **Layout group prediction**
Design for Manufacturing	**Hotspot prediction** **In-design detection and fixing**
PCB Synthesis	**Faster design closure** **Routability**
System Design and Analysis	**Reduction in simulation time**

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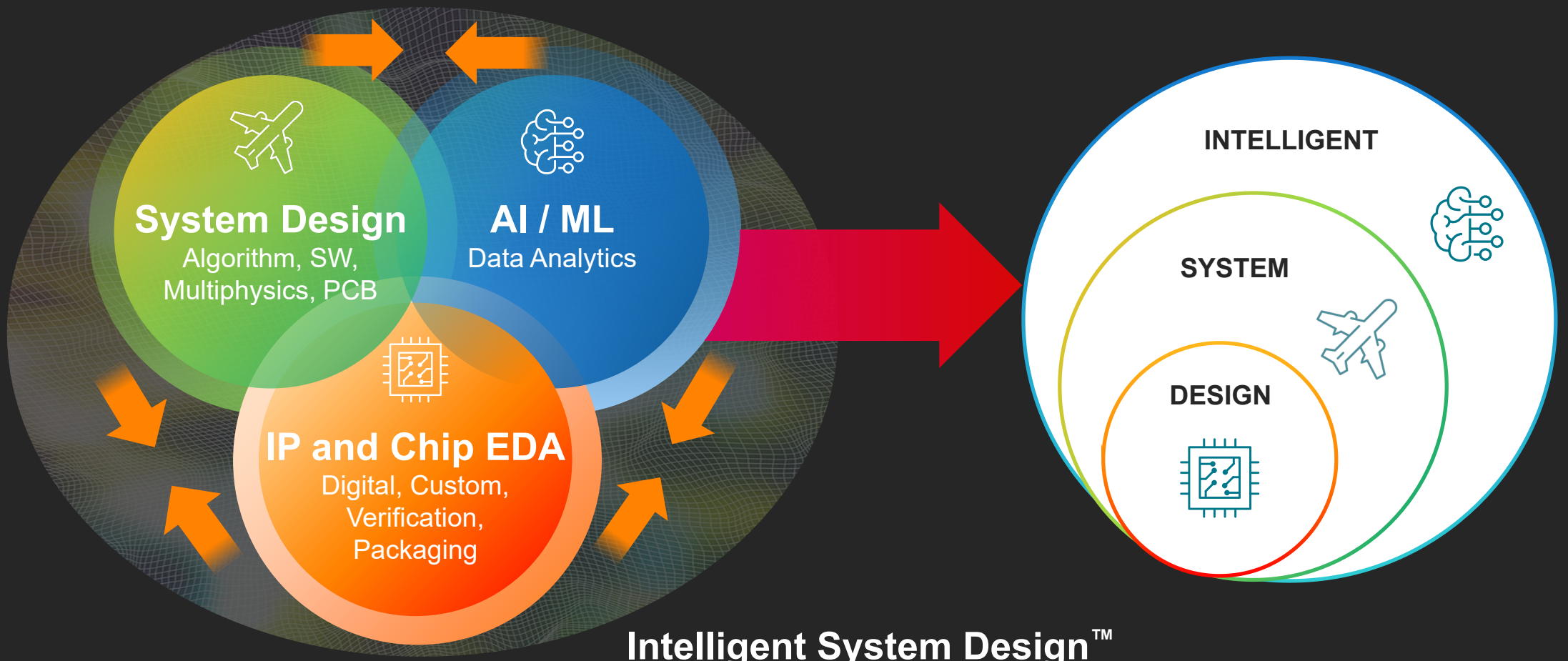
This is truly just the beginning!

Leading the Computational Software Convergence



Intelligent System Design™

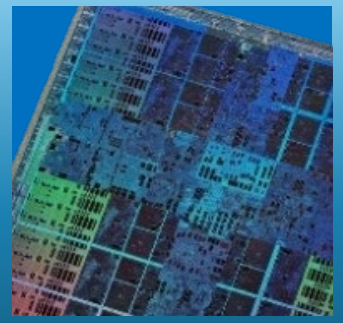
Merger of EDA, system design, AI | Pervasive intelligence throughout design | Grounded in computational engineering

Co-optimizing system, hardware, software | Spanning multiple system domains

Electronics Innovation – An Exiting Future Ahead

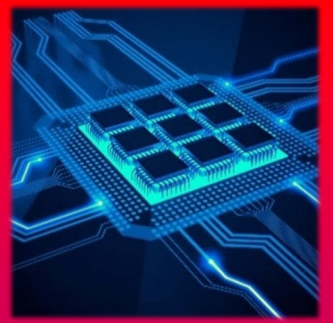
2020's

Edge-to-Cloud and 5G

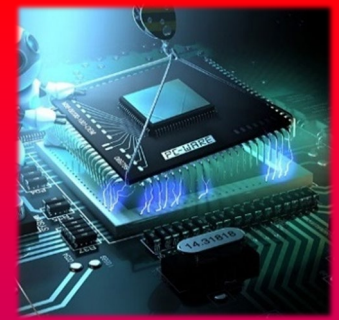


Specialized SoCs

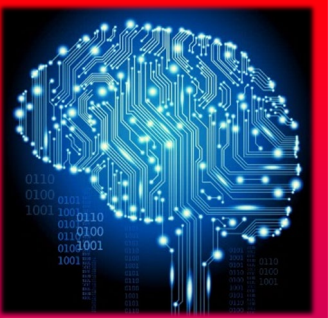
Artificial Intelligence



Parallel and Distributed

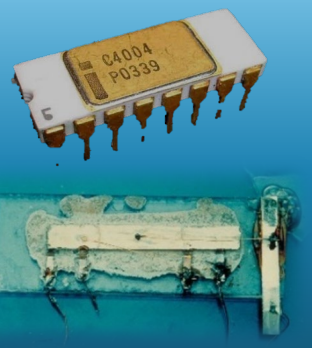


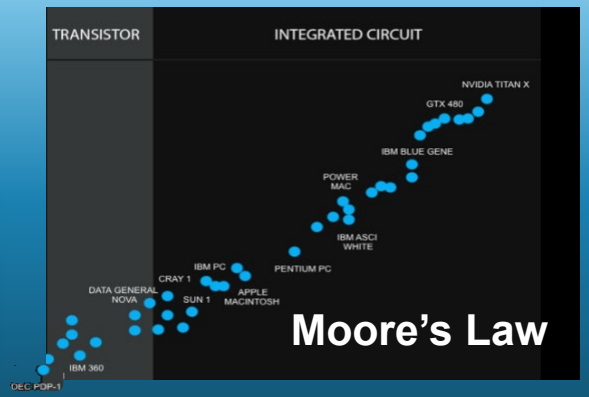
Full-Flow Solutions

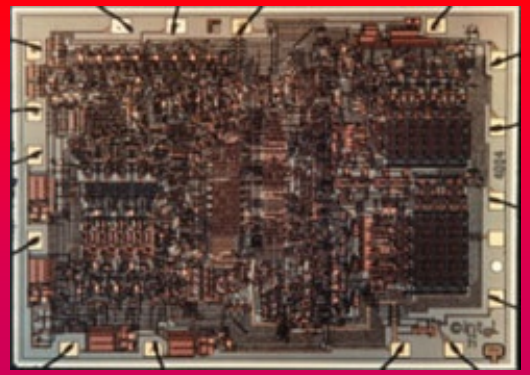


Deep Learning

1960's







Semiconductors and Systems

EDA System Design Enablement